TVP4010
Data Manual

3D Graphics Processor

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1 Introduction

The TVP4010 high-performance 3D graphics processor combines workstation-class 3D graphics acceleration and state of the art 2D performance in a single chip. All 3D rendering operations are accelerated by the TVP4010 including Gouraud shading, depth buffering, texture mapping and alpha blending.

Implemented around a saleable memory architecture, the TVP4010 reduces the cost and complexity of delivering high-performance 3D graphics within a windowing environment making it ideal for a wide range of graphics products from PC boards to workstation accelerators.

The major TVP4010 functional blocks are:

- PCI interface
- Graphics core
- Memory interface
- Video timing generation
- Auxiliary device support
- Reset configuration control
- ROM support
- Address maps

1.1 Features

Texture Mapping

- True per-pixel perspective correction
- High-quality bilinear filtering
- Palletized and RGB textures
- Local texture buffer
- Specular texture highlighting
- Fast texture loading with DMA
- Real-time video textures
- Chroma-keying
- Configurable texture compression

3D Rendering

- Points, lines, triangles and sprites
- Gouraud and flat shading
- Optional Z-buffering (16-bit)
- Fog and depth-cueing
- Blending and stippling
- Volumetric collision detection
- Stencil buffer (1-bit)
- Real-time full scene anti-aliasing
- Scissor test and logic operations
- 3D transparent sprites with Z

Advanced Real-Time 2D Processing

- Fast affine image transforms
- Flexible alpha-based compositing
- Alpha-blended sprites with full Z
- Stencil for cut-outs

GUI Acceleration

- Over 30 million Winmarks (WinBench 97)
- BitBlt with ROPS
- Fast linear addressed framebuffer
- Block fill and text acceleration
- 8-, 16-, and 24-bit color
- Fast on-chip SVGA
- Windows and QuickDraw™ drivers
- Bypass to linear framebuffer

Accelerated Video Playback

- YUV to RGB conversion
- MPEG compatible
- XY scaling and smoothing
- Dithering
- Chroma-keying (with color range)

Performance (TVP4010 – 80)

- 42 M textured pixels/sec
- 800 K textured polygons/sec
- 2 Gbyte/sec block fill
- 120 Mbyte/sec texture download rate
- 30 fps scaled, filtered video playback

Display Features

- Double and triple-buffering
- 32-bit RGBA for 2D
- 16-bit RGBA for 3D
- 8-and 16-bit dithering
- 320 x 200 to 1600 x 1200 resolution
- Hardware pan

PCI Interface

- 32-bit glueless PCI bus (Rev 2.1)
- DMA mastering
- 32-entry command FIFO
- Byte swapping for Mac platforms
- ACI interrupt support
- GLINT Delta interface

Memory Architecture

- 64-bit SGRAM/SDRAM interface
  - SDRAM for lower cost
  - SGRAM for higher performance
- 600 Mbyte/sec bandwidth
- Single 2, 4, 6, or 8 Mbytes total memory
- Multi-function memory store:
  - Display buffer and backbuffer(s)
  - Texture maps
  - Z-buffer and stencil data
- Flexible memory usage
  - Can use rendered images as texture
  - Dynamic allocation of memory
- Linear and patched addressing
- Block and masked writes
- Mixed RGBA, CI and YUV data

System Integration

- 3.3 V supply, 2.5 W
- 256-terminal BGA package
- Internal video timing generator
- Fast 32-bit LUT-DAC port
- ROM interface
- VESA DPMS and DDC

1.2 Functional Block Diagram

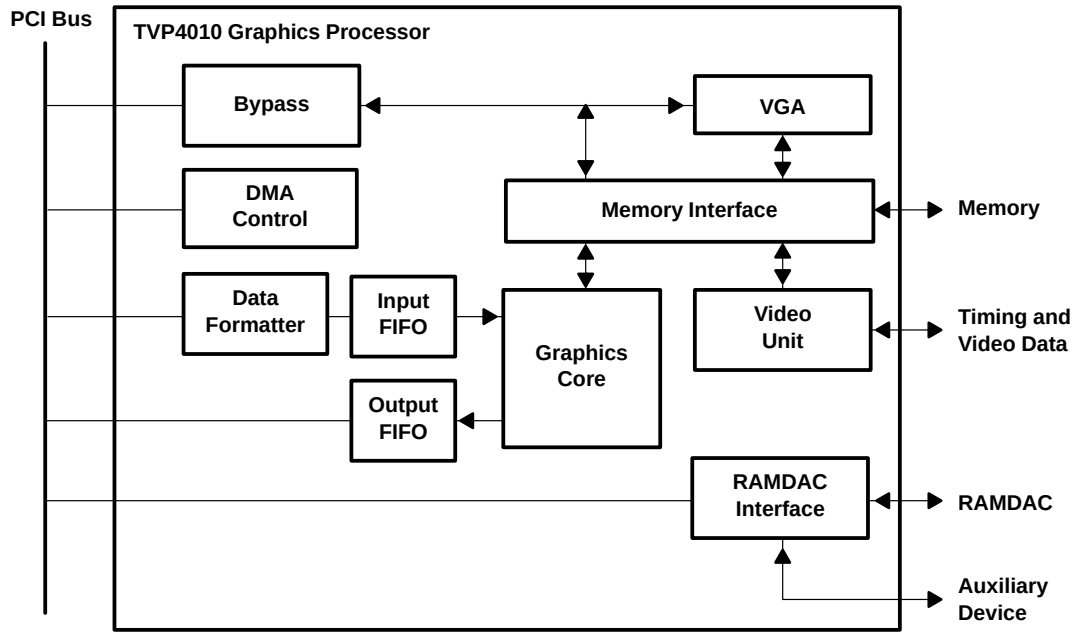


Figure 1–1. Functional Block Diagram

1.3 Terminal Assignments

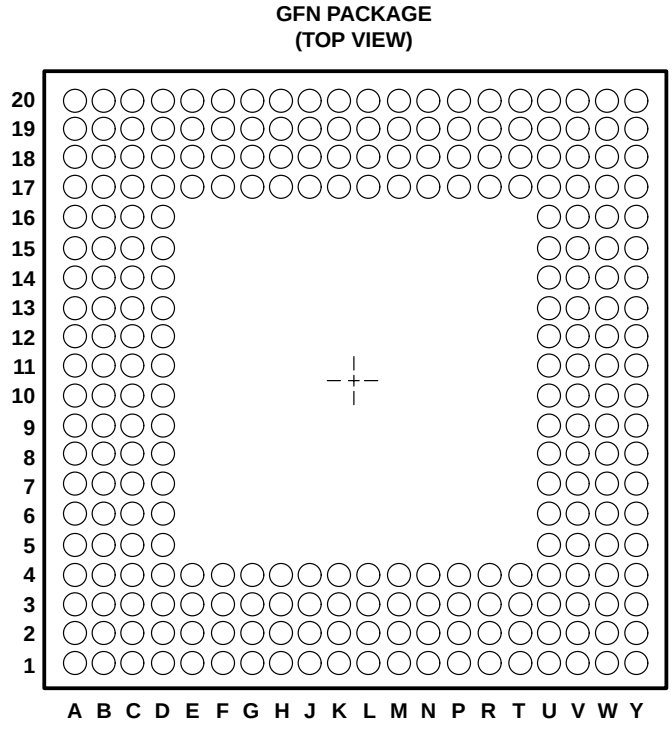


Figure 1–2. Terminal Assignments

1.4 Ordering Information

TVP4010 – XX XXX

Pixel Clock

MUST CONTAIN TWO CHARACTERS:

–60: 60–MHz pixel clock
–80: 80–MHz pixel clock

Package

MUST CONTAIN THREE LETTERS:

GFN: Plastic Ball Grid Array

1.5 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION	DRIVE†
$\overline{\text{AUXREAD}}$	E18	O	Aux read	8
$\overline{\text{AUXWAIT}}$	E17	I	Aux wait	–
$\overline{\text{AUXWRITE}}$	D19	O	Aux write	8
DDC	C19	I	DDC data port	–
MADD0	Y13	O	Memory address	12
MADD1	U12	O	Memory address	12
MADD2	V12	O	Memory address	12
MADD3	W12	O	Memory address	12
MADD4	Y12	O	Memory address	12
MADD5	U11	O	Memory address	12
MADD6	V11	O	Memory address	12
MADD7	W11	O	Memory address	12
MADD8	Y11	O	Memory address	12
MADD9	Y10	O	Memory address	12
MBANK0	J18	O	Memory bank select	8
MBANK1	J19	O	Memory bank select	8
MBANK2	J20	O	Memory bank select	8
MBANK3	K17	O	Memory bank select	8
MBYTE0	J17	O	Memory byte enable	8
MBYTE1	H20	O	Memory byte enable	8
MBYTE2	H19	O	Memory byte enable	8
MBYTE3	H18	O	Memory byte enable	8
MBYTE4	G20	O	Memory byte enable	8
MBYTE5	G19	O	Memory byte enable	8
MBYTE6	F20	O	Memory byte enable	8
MBYTE7	E20	O	Memory byte enable	8
MCAS0	M20	O	Memory byte enable	8
MCAS1	L19	O	Memory byte enable	8
MCLK	B10	I	System clock	–
MDAT0	W3	I/O	Memory data	8
MDAT1	W4	I/O	Memory data	8
MDAT10	W9	I/O	Memory data	8
MDAT11	W10	I/O	Memory data	8
MDAT12	W13	I/O	Memory data	8
MDAT13	Y14	I/O	Memory data	8
MDAT14	Y15	I/O	Memory data	8
MDAT15	Y16	I/O	Memory data	8
MDAT16	V15	I/O	Memory data	8

† Output power ratings are marked as 8 or 12 for the mA current rating, or P indicating a PCI compatible output.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION	DRIVE†
MDAT17	Y17	I/O	Memory data	8
MDAT18	W17	I/O	Memory data	8
MDAT19	U16	I/O	Memory data	8
MDAT2	U5	I/O	Memory data	8
MDAT20	W18	I/O	Memory data	8
MDAT21	V18	I/O	Memory data	8
MDAT22	Y20	I/O	Memory data	8
MDAT23	V19	I/O	Memory data	8
MDAT24	U18	I/O	Memory data	8
MDAT25	V20	I/O	Memory data	8
MDAT26	T18	I/O	Memory data	8
MDAT27	T20	I/O	Memory data	8
MDAT28	P17	I/O	Memory data	8
MDAT29	P18	I/O	Memory data	8
MDAT3	Y4	I/O	Memory data	8
MDAT30	P20	I/O	Memory data	8
MDAT31	N19	I/O	Memory data	8
MDAT32	Y2	I/O	Memory data	8
MDAT33	V4	I/O	Memory data	8
MDAT34	Y3	I/O	Memory data	8
MDAT35	V5	I/O	Memory data	8
MDAT36	Y5	I/O	Memory data	8
MDAT37	U7	I/O	Memory data	8
MDAT38	V7	I/O	Memory data	8
MDAT39	Y7	I/O	Memory data	8
MDAT4	W5	I/O	Memory data	8
MDAT40	W8	I/O	Memory data	8
MDAT41	V9	I/O	Memory data	8
MDAT42	Y9	I/O	Memory data	8
MDAT43	V10	I/O	Memory data	8
MDAT44	V13	I/O	Memory data	8
MDAT45	W14	I/O	Memory data	8
MDAT46	V14	I/O	Memory data	8
MDAT47	U14	I/O	Memory data	8
MDAT48	W16	I/O	Memory data	8
MDAT49	V16	I/O	Memory data	8
MDAT5	V6	I/O	Memory data	8
MDAT50	Y18	I/O	Memory data	8

† Output power ratings are marked as 8 or 12 for the mA current rating, or P indicating a PCI compatible output.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION	DRIVE†
MDAT51	V17	I/O	Memory data	8
MDAT52	Y19	I/O	Memory data	8
MDAT53	W19	I/O	Memory data	8
MDAT54	W20	I/O	Memory data	8
MDAT55	U19	I/O	Memory data	8
MDAT56	T17	I/O	Memory data	8
MDAT57	U20	I/O	Memory data	8
MDAT58	T19	I/O	Memory data	8
MDAT59	R18	I/O	Memory data	8
MDAT6	W6	I/O	Memory data	8
MDAT60	R19	I/O	Memory data	8
MDAT61	P19	I/O	Memory data	8
MDAT62	N18	I/O	Memory data	8
MDAT63	N20	I/O	Memory data	8
MDAT7	W7	I/O	Memory data	8
MDAT8	V8	I/O	Memory data	8
MDAT9	Y8	I/O	Memory data	8
MDSF0	K18	O	Memory DSF	8
MDSF1	K20	O	Memory DSF	8
MEMCKE	G17	O	Memory clock enable	8
MEMCKOUT0	F18	O	Memory clock	12
MEMCKOUT1	E19	O	Memory clock	12
MRAS0	M18	O	Memory RAS	8
MRAS1	M19	O	Memory RAS	8
MWE0	L18	O	Memory write enable	8
MWE1	L20	O	Memory write enable	8
NC0	A15	I	No connection (see Note 1)	–
NC2	F19	I	No connection (see Note 1)	–
NC4	R20	I	No connection (see Note 1)	–
NC5	W15	I	No connection (see Note 1)	–
NC6	Y6	I	No connection (see Note 1)	8
PCIAD0	Y1	I/O	PCI address and data	P
PCIAD1	W1	I/O	PCI address and data	P
PCIAD10	R1	I/O	PCI address and data	P
PCIAD11	R3	I/O	PCI address and data	P
PCIAD12	P1	I/O	PCI address and data	P
PCIAD13	P2	I/O	PCI address and data	P

† Output power ratings are marked as 8 or 12 for the mA current rating, or P indicating a PCI compatible output.
NOTE 1: Unused terminals should be left no connect.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION	DRIVE†
PCIAD14	P3	I/O	PCI address and data	P
PCIAD15	P4	I/O	PCI address and data	P
PCIAD16	L1	I/O	PCI address and data	P
PCIAD17	L2	I/O	PCI address and data	P
PCIAD18	K1	I/O	PCI address and data	P
PCIAD19	K3	I/O	PCI address and data	P
PCIAD2	W2	I/O	PCI address and data	P
PCIAD20	J1	I/O	PCI address and data	P
PCIAD21	J2	I/O	PCI address and data	P
PCIAD22	J3	I/O	PCI address and data	P
PCIAD23	J4	I/O	PCI address and data	P
PCIAD24	F2	I/O	PCI address and data	P
PCIAD25	G2	I/O	PCI address and data	P
PCIAD26	G3	I/O	PCI address and data	P
PCIAD27	F3	I/O	PCI address and data	P
PCIAD28	G4	I/O	PCI address and data	P
PCIAD29	E1	I/O	PCI address and data	P
PCIAD3	V1	I/O	PCI address and data	P
PCIAD30	E2	I/O	PCI address and data	P
PCIAD31	E3	I/O	PCI address and data	P
PCIAD4	V2	I/O	PCI address and data	P
PCIAD5	V3	I/O	PCI address and data	P
PCIAD6	U2	I/O	PCI address and data	P
PCIAD7	T1	I/O	PCI address and data	P
PCIAD8	T3	I/O	PCI address and data	P
PCIAD9	T4	I/O	PCI address and data	P
PCICBEN0	T2	I/O	PCI byte enable	P
PCICBEN1	N2	I/O	PCI byte enable	P
PCICBEN2	L3	I/O	PCI byte enable	P
PCICBEN3	G1	I/O	PCI byte enable	P
PCICLK	C4	I	PCI clock	–
$\overline{\text{PCIDEVSEL}}$	M3	I/O	PCI device select	P
PCIFIFOINDIS	C2	O	Delta control	P
PCIFIFOOUTDILS	D2	O	Delta control	P
$\overline{\text{PCIFRAME}}$	L4	I/O	PCI frame	P
$\overline{\text{PCIGNT}}$	A2	I	PCI grant	–
PCIIDSEL	H1	I	PCI id	–

† Output power ratings are marked as 8 or 12 for the mA current rating, or P indicating a PCI compatible output.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION	DRIVE†
$\overline{\text{PCIINTA}}$	B1	OD‡	PCI interrupt	P
$\overline{\text{PCIIRDY}}$	M1	I/O	PCI ready	P
PCIPAR	N1	I/O	PCI parity	P
$\overline{\text{PCIREQ}}$	C1	O	PCI request	P
$\overline{\text{PCIRST}}$	C3	I	PCI reset	–
$\overline{\text{PCISTOP}}$	M4	I/O	PCI stop	P
$\overline{\text{PCITRDY}}$	M2	I/O	PCI ready	P
$\overline{\text{RAMDACR}}$	C20	O	RAMDAC read	8
$\overline{\text{RAMDACW}}$	D18	O	RAMDAC write	8
RDACADD0	A20	O	RAMDAC address	8
RDACADD1	B19	O	RAMDAC address	8
RDACADD2	C18	O	RAMDAC address	8
RDACADD3	B20	O	RAMDAC address	8
RDACDAT0	B16	I/O	RAMDAC data	8
RDACDAT1	C16	I/O	RAMDAC data	8
RDACDAT2	A17	I/O	RAMDAC data	8
RDACDAT3	A18	I/O	RAMDAC data	8
RDACDAT4	D16	I/O	RAMDAC data	8
RDACDAT5	C17	I/O	RAMDAC data	8
RDACDAT6	B17	I/O	RAMDAC data	8
RDACDAT7	B18	I/O	RAMDAC data	8
RESERVED0	E4	I	No connection (see Note 1)	–
RESERVED1	D5	I	No connection (see Note 1)	–
RESERVED2	B2	I	No connection (see Note 1)	–
RESETOUT	A19	O	External reset	8
RI	C5	I	Pull high (see Note 2)	–
$\overline{\text{ROM}}$	D20	O	ROM enable	8
$\overline{\text{ROMWE}}$	D3	O	ROM write enable	8
TEST2	K19	I	No connection (see Note 1 and Note 2)	–
TESTACLK	G18	I	No connection (see Note 1 and Note 2)	–
TESTCCLK	M17	I	No connection (see Note 1 and Note 2)	–
TESTGCLK	H2	I	No connection (see Note 1 and Note 2)	–
TESTMODE	U9	I	Pull low (see Note 2)	–
V_{CC0}	F1		Supply voltage	–
V_{CC1}	R2		Supply voltage	–

† Output power ratings are marked as 8 or 12 for the mA current rating, or P indicating a PCI compatible output.
‡ OD is open drain.

NOTES: 1. Unused terminals should be left no connect.
2. Test terminal RI should be pulled high in functional mode, test terminal TESTMODE should be tied low, all other test terminals (TESTACLK, TESTBCLK, TESTCCLK, TESTGCLK) should be left no connect.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION	DRIVE†
VCLK	A3	I	Video clock	–
V_{DD0}	D11		Supply voltage	–
V_{DD1}	D15		Supply voltage	–
V_{DD10}	U15		Supply voltage	–
V_{DD11}	U6		Supply voltage	–
V_{DD2}	D6		Supply voltage	–
V_{DD3}	F17		Supply voltage	–
V_{DD4}	F4		Supply voltage	–
V_{DD5}	K4		Supply voltage	–
V_{DD6}	L17		Supply voltage	–
V_{DD7}	R17		Supply voltage	–
V_{DD8}	R4		Supply voltage	–
V_{DD9}	U10		Supply voltage	–
VGAACTIVE	B4	O	Video is from VGA	8
VIDBLANK	B5	O	Video blank	8
VIDCTL0	B3	O	Control for clock synthesizer	8
VIDCTL1	A4	O	Control for clock synthesizer	8
VIDHSYNC	D7	O	Video horizontal sync	8
VIDPIX0	A5	O	Pixel data	8
VIDPIX1	B6	O	Pixel data	8
VIDPIX10	C9	O	Pixel data	8
VIDPIX11	B9	O	Pixel data	8
VIDPIX12	A9	O	Pixel data	8
VIDPIX13	D10	O	Pixel data	8
VIDPIX14	A10	O	Pixel data	8
VIDPIX15	A11	O	Pixel data	8
VIDPIX16	C11	O	Pixel data	8
VIDPIX17	B11	O	Pixel data	8
VIDPIX18	A12	O	Pixel data	8
VIDPIX19	B12	O	Pixel data	8
VIDPIX2	C7	O	Pixel data	8
VIDPIX20	C12	O	Pixel data	8
VIDPIX21	D12	O	Pixel data	8
VIDPIX22	A13	O	Pixel data	8
VIDPIX23	B13	O	Pixel data	8
VIDPIX24	C13	O	Pixel data	8
VIDPIX25	A14	O	Pixel data	8
VIDPIX26	B14	O	Pixel data	8

† Output power ratings are marked as 8 or 12 for the mA current rating, or P indicating a PCI compatible output.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION	DRIVE†
VIDPIX27	C14	O	Pixel data	8
VIDPIX28	B15	O	Pixel data	8
VIDPIX29	D14	O	Pixel data	8
VIDPIX3	A6	O	Pixel data	8
VIDPIX30	C15	O	Pixel data	8
VIDPIX31	A16	O	Pixel data	8
VIDPIX4	B7	O	Pixel data	8
VIDPIX5	A7	O	Pixel data	8
VIDPIX6	C8	O	Pixel data	8
VIDPIX7	B8	O	Pixel data	8
VIDPIX8	A8	O	Pixel data	8
VIDPIX9	D9	O	Pixel data	8
VIDVSYNC	C6	O	Video vertical sync	8
V_{SS0}	A1		Ground (see Note 3)	–
V_{SS1}	C10		Ground (see Note 3)	–
V_{SS10}	K2		Ground (see Note 3)	–
V_{SS11}	N17		Ground (see Note 3)	–
V_{SS12}	N3		Ground (see Note 3)	–
V_{SS13}	N4		Ground (see Note 3)	–
V_{SS14}	U1		Ground (see Note 3)	–
V_{SS15}	U13		Ground (see Note 3)	–
V_{SS16}	U17		Ground (see Note 3)	–
V_{SS17}	U3		Ground (see Note 3)	–
V_{SS18}	U4		Ground (see Note 3)	–
V_{SS19}	U8		Ground (see Note 3)	–
V_{SS2}	D1		Ground (see Note 3)	–
V_{SS3}	D13		Ground (see Note 3)	–
V_{SS4}	D17		Ground (see Note 3)	–
V_{SS5}	D4		Ground (see Note 3)	–
V_{SS6}	D8		Ground (see Note 3)	–
V_{SS7}	H17		Ground (see Note 3)	–
V_{SS8}	H3		Ground (see Note 3)	–
V_{SS9}	H4		Ground (see Note 3)	–

† Output power ratings are marked as 8 or 12 for the mA current rating, or P indicating a PCI compatible output.
NOTE 3: All V_{SS} terminals must be connected to ground, including the central terminal grid H8–N13.

2 Detailed Description

2.1 PCI Interface

The PCI interface conforms to the PCI local bus standard revision 2.1. The TVP4010 is a PCI local bus target and a PCI local bus read master.

The PCI interface has an input FIFO for passing data to the graphics core, and an output FIFO for buffering up data to be read from the graphics core. The input FIFO is 32 words deep; the output FIFO is 8 words deep. A DMA controller is provided in the PCI interface to allow the TVP4010 to read data directly into the graphics core input FIFO.

2.2 Graphics Core

The graphics core in the TVP4010 accelerates the key operations for 3D and 2D applications. For further information on the functionality of the graphics core refer to the TVP4010 Programmer's Reference Manual.

2.3 Memory Interface

The local memory is used to store color, depth, stencil, and texture data. For more information on the different data types and their usage refer to the TVP4010 Programmers Reference Manual.

The memory is organized as 1 to 4 banks of synchronous graphics RAM (SGRAM). Each bank is 64 bits wide and made up of two devices, each 32 bits wide by 256K entries deep. This gives 2 Mbytes per bank, with a maximum memory array of 8 Mbytes.

Bank zero must always be fitted since the VGA uses this area for local storage. Any other combination of banks may be fitted, but for contiguous memory banks should be added from 1 to 3.

The TVP4010 makes use of special SGRAM features including block fill and write-per-bit masking. SDRAM may be used in place of SGRAM if it is identical to SGRAM except for missing block write and write per bit masks.

2.4 Video Timing Generation

The TVP4010 has an internal timing generator. The maximum video clock (VCLK) is 50 MHz. Absolute maximum TVP4010 video clock rates are shown in Table 2–1.

Table 2–1. Maximum Pixel Clock Frequencies

PIXEL WIDTH	MAXIMUM PIXEL FREQUENCY
32 bit	50 MHz
16 bit	100 MHz
8 bit	200 MHz

2.5 Auxiliary Device Support

The TVP4010 can act as a gateway to an additional device which shares address and data lines with the RAMDAC. This device can be mapped into I/O space as well as memory space. The auxiliary bus protocol is asynchronous and supports a wait signal that the slave device may use to insert wait states into a transaction.

2.6 Reset Configuration Control

A number of parameters for the TVP4010 are set at reset time, such as memory size and speed. The reset state is configured with resistors connected to the memory and video port data terminals. The state of the data terminals is sampled on the rising edge of the reset line. See Section 2.23, *Reset Control* for more details.

2.7 ROM Support

The TVP4010 supports a flash ROM. This ROM may store code needed for device-specific initialization and the VGA BIOS.

2.8 Address Mapping

The TVP4010 has seven PCI base address regions as listed in Table 2–2.

Table 2–2. PCI Address Regions

REGION	DESCRIPTION
Configuration	PCI configuration region
0	GC control region
1	Bypass access to memory
2	Bypass access to memory
3	Auxiliary bus
4	Delta aperture
ROM	Expansion ROM

Two memory apertures are provided, each is a PCI region with a fixed size of 8 Mbytes. A variety of access modes are available, including byte swapped, half-word swapped, and packed 16-bit pixel modes to support per-window double buffering with a suitable RAMDAC. Each aperture can be programmed to address the memory controller directly, or to address the memory through the VGA subsystem. The two separately controlled apertures allow different views of the memory to co-exist without register reprogramming; for example, one aperture could be set for local buffer data accesses and the other for frame buffer data accesses.

The two memory apertures can also be programmed to allow reading and writing of the ROM instead of memory. This ensures that the ROM is visible beyond system boot time, making it possible to program a flash ROM device in the system.

When displaying images in 16-bit per-window double buffered mode the frame buffer area of memory is divided into two interleaved buffers, A and B. Each pixel uses 32 bits: the bottom 16 bits (0–15) form buffer A, and the top 16 bits (16–31) form buffer B. The top bit in buffer B is used by the RAMDAC to select which buffer is displayed, on a per–pixel basis.

The control registers for each of memory apertures one and two can be set to allow reading and writing of buffers A and B as contiguous 16-bit packed buffers although they are pixel interleaved in the memory. Each 32-bit read or write access over the PCI bus thus transfers two pixels to/from the selected 16-bit packed buffer. The apertures can be programmed to access either buffer A or buffer B, to write to both buffer A and buffer B, or to read from the active buffer as specified by bit 31.

A further control bit is provided to route the memory address via the VGA controller, rather than directly to the main memory controller. This allows the memory address to be interpreted as a VGA address. This mechanism allows the VGA to be relocated away from the standard fixed addresses. The fixed addresses may be optionally disabled so that two VGA systems can co-exist on the same bus.

2.9 Test Mode

When the conditions listed in Table 2–3 are met, the TVP4010 will go to in-circuit test mode.

Table 2–3. Test Mode

TERMINAL	NAME	STATE
U9	TESTMODE	High
E17	AUXWAITN	Low
C19	DDC	Low

2.10 PCI Configuration

2.10.1 PCI Configuration Region

The PCI configuration region provides information that satisfies the needs of current and anticipated system configuration mechanisms.

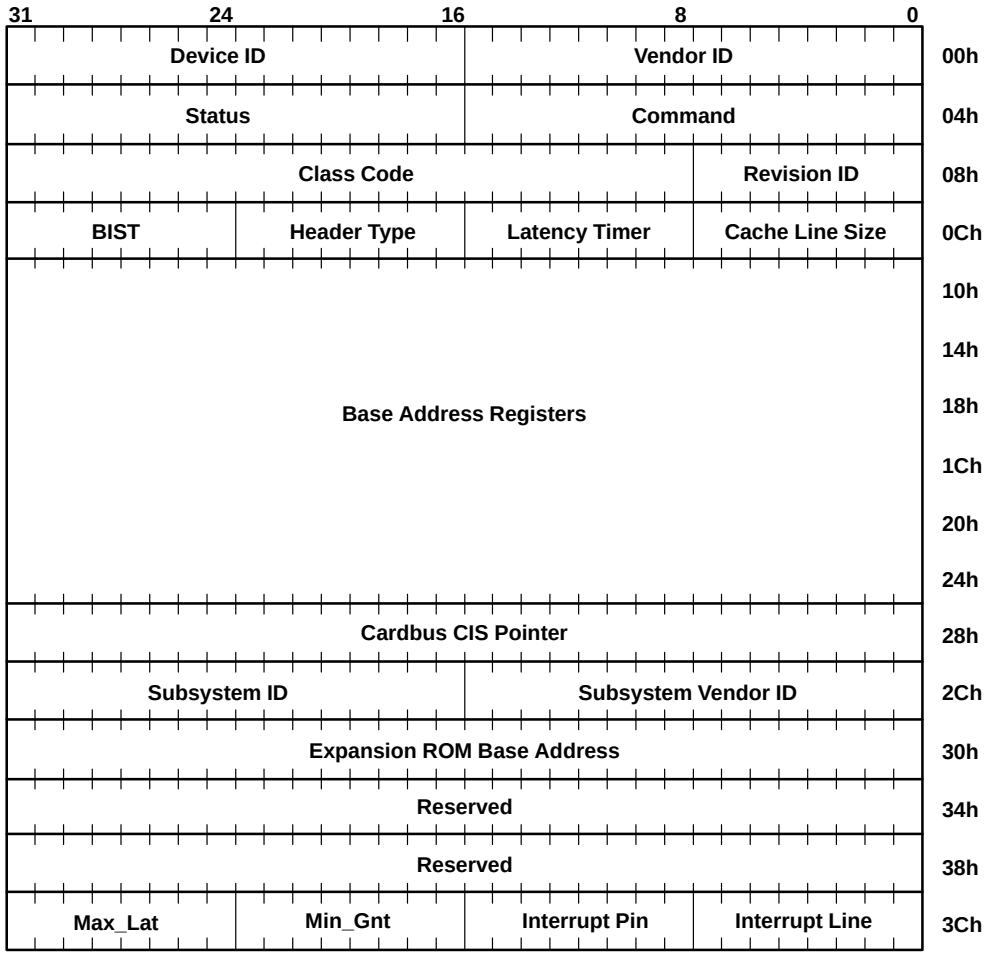


Figure 2–1. PCI Configuration Region

2.11 PCI Register Set

For more information about the use of the registers in this section refer to the PCI specification.

2.11.1 Vendor ID Register (CFGVendorId) (Region: Configuration, Index: 0x00, Access: R, Default: 0x104C)

The vendor identification register contains the vendor identification number or Texas Instruments company code.

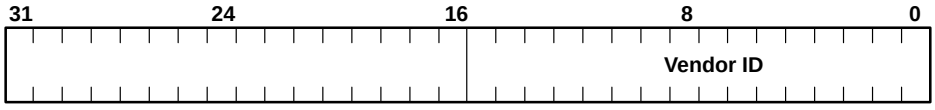


Table 2–4. Vendor ID Register

NAME	DESCRIPTION
Bits 0–15	0x104C

2.11.2 Device ID Register (CFGDeviceId) (Region: Configuration, Index: 0x02, Access: R, Default: 0x3D04)

The device identification register contains the device identification number or TVP4010 device number.

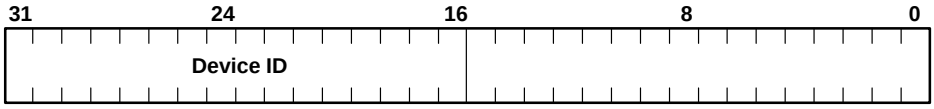


Table 2–5. Device ID Register

NAME	DESCRIPTION
Bits 16–31	0x3D04

2.11.3 Command Register (CFGCommand) (Region: Configuration, Index: 0x04, Access: R/W, Default: 0x00)

The command register provides control over a device's ability to generate and respond to PCI cycles. Writing zero to this register disconnects the device from the PCI for all except configuration accesses. The TVP4010 supports all necessary bits within the command register for the functionality it contains.

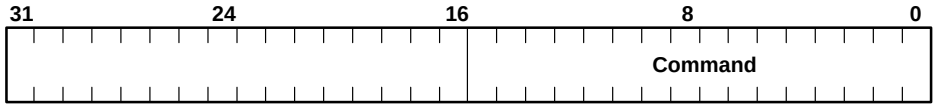


Table 2–6. Command Register

NAME	DESCRIPTION	
Bit 0	I/O space enable	0 = Disable I/O space accesses
		1 = Enable I/O space accesses. If fixed VGA addressing is disabled this bit will be 0 (read-only)
Bit 1	Memory space enable	0 = Disable memory space accesses
		1 = Enable memory space accesses
Bit 2	Bus master enable	0 = Disable master accesses
		1 = Enable master accesses
Bit 3	Special cycle enable (read only)	0 = TVP4010 never responds to special cycle accesses
Bit 4	Memory write and invalidate Enable	0 = "Memory Write and Invalidate" is never generated
Bit 5	VGA palette snoop enable	0 = Treat palette accesses like all other VGA accesses
		1 = Enable VGA palette snooping. If fixed VGA addressing is disabled, this bit is 0.
Bit 6	Parity error response enable (read only)	0 = TVP4010 does not support parity error reporting
Bit 7	Address/data stepping enable (read only)	0 = TVP4010 does not perform stepping
Bit 8	SERR driver enable (read only)	0 = TVP4010 does not support parity error reporting
Bit 9	Master fast back-to-back enable (read only)	0 = The TVP4010 master does not do fast back-to-back access
Bits 10–15	Reserved (read only) default = 000000b	

2.11.4 Status Register (CFGStatus) (Region: Configuration, Index: 0x06, Access: R, Default: 0x00)

Writes to this register cause bits to be reset, but not set. A bit is reset whenever the register is loaded with the corresponding bit position set to one.

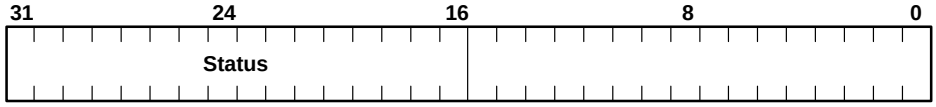


Table 2–7. Status Register

NAME	DESCRIPTION	
Bits 0–4	Reserved (read only). Default = 00000b.	
Bit 5	66 MHz capable (read only)	0 = TVP4010 is 33 MHz capable only
Bit 6	UDF supported (read only)	0 = TVP4010 does not support user-definable configurations
Bit 7	Fast back-to-back capable (read only)	1 = TVP4010 can accept fast back-to-back PCI transactions
Bit 8	Data parity error detected (read only)	0 = Parity checking not implemented on TVP4010
Bits 9–10	DEVSEL timing (read only)	01b = TVP4010 asserts DEVSEL# at medium speed
Bit 11	Signalled target abort (read only)	0 = TVP4010 never signals target-abort
Bit 12	Received target abort. This bit is set by the TVP4010 bus master whenever its transaction is terminated with target-abort.	
Bit 13	Received master abort. This bit is set by the TVP4010 bus master when ever its transaction is terminated with master-abort.	
Bit 14	Signalled system error (read only)	0 = TVP4010 never asserts a system error
Bit 15	Detected parity error (read only)	0 = Parity checking is not implemented by the TVP4010

2.11.5 Revision ID Register (CFGRevisionId) (Region: Configuration, Index: 0x08, Access: R, Default: Rev Number)

The revision identification register identifies the revision identification number.

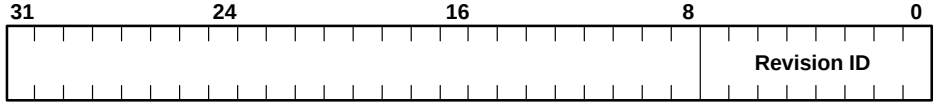


Table 2–8. Revision ID Register

NAME	DESCRIPTION
Bits 0–7	Revision A, default = 0x01

2.11.6 Class Code Register (CFGClassCode) (Region: Configuration, Index: 0x09, Access: R, Default: Config Data)

The class code register identifies the generic function of the TVP4010, which depends on the setting of configuration data detailed below.

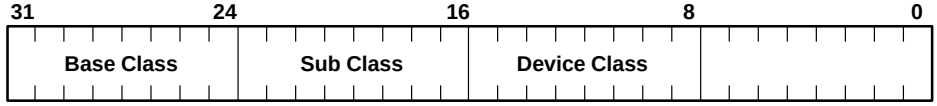


Table 2–9. Class Code Register

NAME	DESCRIPTION
Bits 8–15	Device class, 00h (see table below)
Bits 16–23	Sub class, 80h (see table below)
Bits 24–31	Base class, 03h (see table below)

Table 2–10. Class Code Register Configuration

BASECLASSZERO (CONFIG BIT)	FIXED VGA ADDRESSING	BASE CLASS	SUB CLASS	DEVICE CLASS	MEANING (SEE PCI SPEC APPENDIX D)
0	Disabled	03h	80h	00h	Other display controller
0	Enabled	03h	01h	00h	VGA-compatible controller
1	Disabled	00h	00h	00h	Non VGA-compatible device
1	Enabled	00h	01h	00h	VGA-compatible device

2.11.7 Cache Line Size Register (CFGCacheLine) (Region: Configuration, Index: 0x0C, Access: R, Default: 0x00)

The cache line size register specifies the cache line size in units of 32-bit words. It is only implemented for masters which use the memory write and invalidate command. The TVP4010 does not use this command.

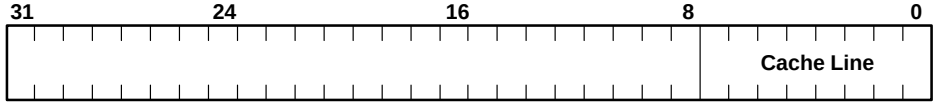


Table 2–11. Cache Line Size Register

NAME	DESCRIPTION
Bits 0–7	Cache line size. Cache line size unsupported. Default = 0x00.

2.11.8 Latency Timer Register (CFGLatTimer) (Region: Configuration, Index: 0x0D, Access: R/W, Default: 0x00)

The latency timer register specifies, in PCI bus clocks, the value of the latency timer for this PCI bus master.

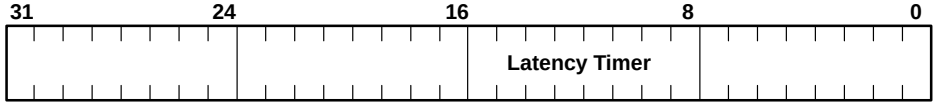


Table 2–12. Legacy Timer Register

NAME	DESCRIPTION
Bits 8–15	Latency timer count. Sets the maximum number of PCI clock cycles for master burst accesses.

2.11.9 Header Type Register (CFGHeaderType) (Region: Configuration, Index: 0x0E, Access: R, Default: 0x00)

The header type register identifies the header type. PCI definition: Single function device.

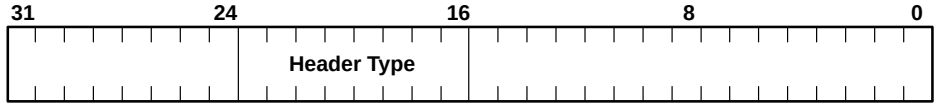


Table 2–13. Header Type Register

NAME	DESCRIPTION
Bits 16–23	0x00

2.11.10 BIST Register (CFGBist) (Region: Configuration, Index: 0x0F, Access: R, Default: 0x00)

The BIST register is optional and is used for control and status of BIST. BIST is unsupported by the TVP4010 over the PCI interface.

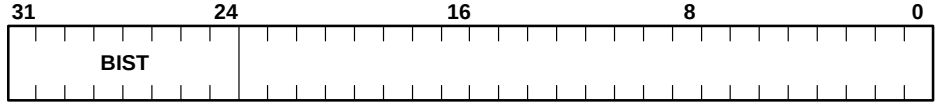


Table 2–14. BIST Register

NAME	DESCRIPTION
Bits 24–31	0x00

2.11.11 Base Address 0 Register (CFGBaseAddr0) (Region: Configuration, Index: 0x10, Access: R/W, Default: 0x00000000)

The base address 0 register contains the TVP4010 control space offset. The control registers are in memory space. They are not prefetchable and can be located anywhere in 32-bit address space.

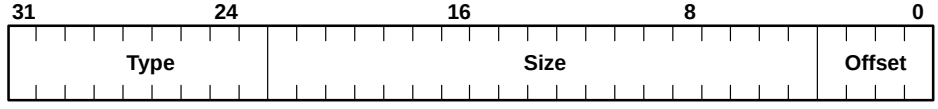


Table 2–15. Base Address 0 Register

NAME	DESCRIPTION
Bits 0–3	Address type (read only). Memory space, not prefetchable, in 32-bit address space. 0h.
Bits 4–16	Size indication (read only). Indicates that the control registers must be mapped into 128 KBytes. 000h.
Bits 17–31	Base offset loaded at boot time to set offset of the control register space.

2.11.12 Base Address 1 Register (CFGBaseAdd1) (Region: Configuration, Index: 0x14, Access: R/W, Default: 0x00000000)

The base address 1 register contains the TVP4010 aperture one memory offset. It is not prefetchable and can be located anywhere in 32-bit address space.

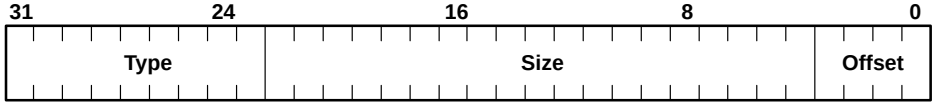


Table 2–16. Base Address 1 Register

NAME	DESCRIPTION
Bit 0–3	Address type (read only). Memory Space, not prefetchable, in 32-bit address space. 0h.
Bits 4–22	Size indication (read only). Fixed at 8 Mbytes.
Bits 23–31	Base offset loaded at boot time to set offset of the memory space.

2.11.13 Base Address 2 Register (CFGBaseAddr2) (Region: Configuration, Index: 0x18, Access: R/W, Default: 0x00000000)

The base address 2 register contains the TVP4010 aperture two memory offset. It is not prefetchable and can be located anywhere in 32-bit address space.

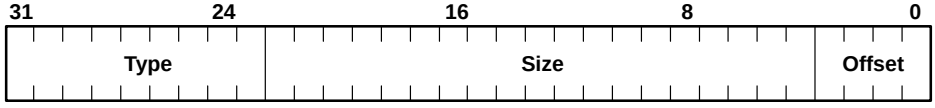


Table 2–17. Base Address 2 Register

NAME	DESCRIPTION
Bits 0–3	Address type (read only). Memory Space, not prefetchable, in 32-bit address space. 0h.
Bits 4–22	Size indication (read only). Fixed at 8 Mbytes.
Bits 23–31	Base offset loaded at boot time to set offset of the memory space.

2.11.14 Base Address 3 Register (CFGBaseAddr3) (Region: Configuration, Index: 0x1C, Access: R/W, Default: Configured)

The base address 3 register contains the base address of the auxiliary bus. This register region is in PCI I/O space, and is enabled by the AuxEnable and AuxIOEnable configuration bits. When not enabled, the base address 3 register is zero and read-only.

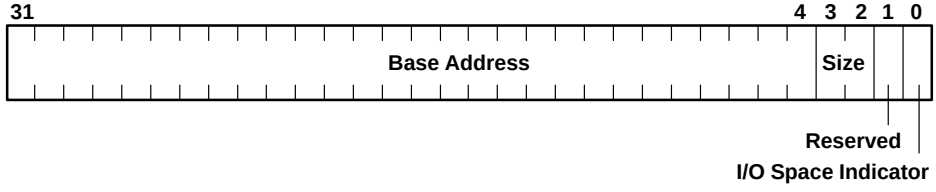


Table 2–18. Base Address 3 Register

NAME	DESCRIPTION	
Bit 0	I/O space indicator (read only)	1 = Region is in PCI I/O Space
Bit 1	Reserved (read only). 0 = Reserved.	
Bits 2–3	Size indication (read only). These bits are zero, giving a region size of 16 bytes.	
Bits 4–31	Base address loaded at boot time to set base address of PCI region three.	

2.11.15 Base Address 4 Register (CFGBaseAddr4) (Region: Configuration, Index: 0x20, Access: R/W, Default: Configured)

The base address 4 register contains the base address of the dummy 256K address region which should be enabled when the TVP4010 is used with a GLINT delta device. This register is enabled by the DeltaEnable configuration bit. When not enabled, the base address 4 register is zero and read-only.

Although the BIOS will allocate a 256K memory region and initialize the base address 4 register, the TVP4010 will never respond to accesses in this allocated memory region. The sole purpose of this register is to obtain a 256K section of the system memory map, which can be used to reposition the GLINT delta base address registers.

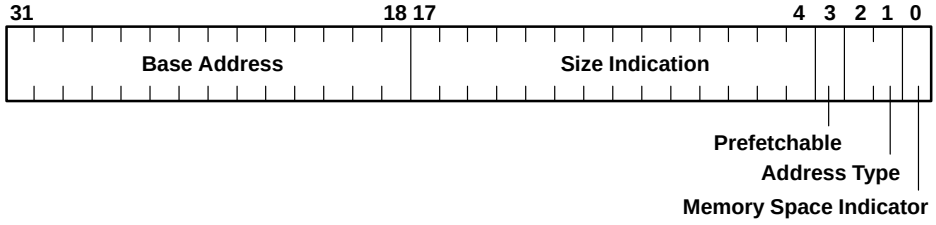


Table 2–19. Base Address 4 Register

NAME	DESCRIPTION	
Bit 0	Memory space indicator (read only)	0 = Region is in PCI memory space
Bits 1–2	Address type (read only)	00b = Locate anywhere in 32–bit address space
Bit 3	Prefetchable (read only)	0 = Region is not prefetchable
Bits 4–17	Size indication (read only). These bits are zero, giving a region size of 256 bytes.	
Bits 18–31	Base address loaded at boot time to set base address of PCI region four.	

2.11.16 CardBus CIS Pointer Register (CFGCardBus) (Region: Configuration, Index: 0x28, Access: R, Default: 0x00)

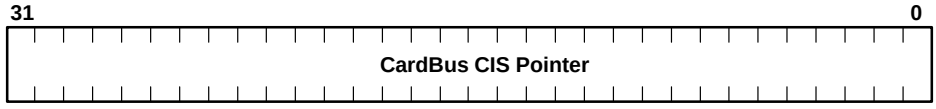


Table 2–20. CardBus CIS Pointer Register

NAME	DESCRIPTION
Bits 0–31	Cardbus pointer. 00000000h = Not implemented

2.11.17 Subsystem Vendor ID Register (CFGSubsystemVendorId) (Region: Configuration, Index: 0x2C, Access: Write Once, Default: 0x0000)

The subsystem vendor ID register is used to identify the vendor of the add-in board on which the TVP4010 device resides. It has a reset value of zero and can only be written to once; all subsequent writes are discarded. All bytes of this register should be initialized by the TVP4010 BIOS after a reset.

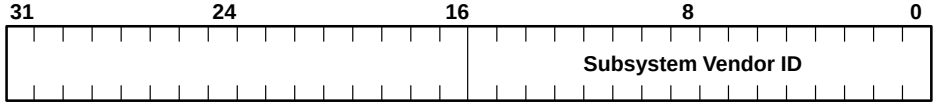


Table 2–21. Subsystem Vendor ID Register

NAME	DESCRIPTION
Bits 0–15	Subsystem vendor ID

2.11.18 Subsystem ID Register (CFGSubsystemId) (Region: Configuration, Index: 0x2E, Access: Write Once, Default: 0x0000)

The subsystem ID register is used to identify the add-in board on which the TVP4010 device resides. It has a reset value of zero, and can only be written to once; all subsequent writes are discarded. Both bytes of this register should be initialized by the TVP4010 BIOS after a reset.

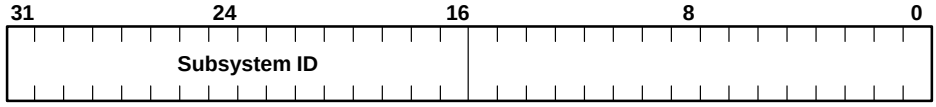


Table 2–22. Subsystem ID Register

NAME	DESCRIPTION
Bits 16–31	Subsystem ID

2.11.19 Expansion ROM Base Address Register (CFGRomAddr) (Region: Configuration, Index: 0x30, Access: R/W, Default: 0x00000000)

The expansion ROM base register is the offset address for the expansion ROM. The ROM is in memory space.

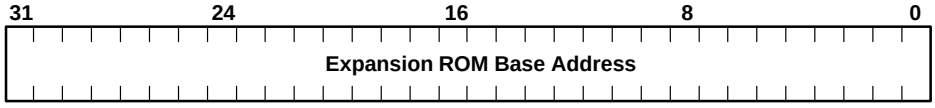


Table 2–23. Expansion ROM Base Address Register

NAME	DESCRIPTION	
Bit 0	Access enable	0 = Expansion ROM accesses disabled
		1 = Expansion ROM accesses enabled
Bit 1	Reserved (read only). PCI reserved register bits.	0x000
Bits 11–15	Size indication (read only). Indicates that the control registers must be mapped into 64 KBytes.	0x00
Bits 16–31	Base offset loaded at boot time to set offset of the expansion ROM.	

2.11.20 Interrupt Line Register (CFGIntLine) (Region: Configuration, Index: 0x3C, Access: R/W, Default: 0x00)

The interrupt line register is an 8-bit register used to communicate interrupt line routing information.

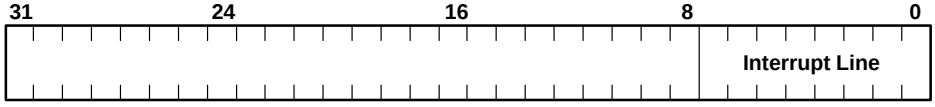


Table 2–24. Interrupt Line Register

NAME	DESCRIPTION
Bits 0–7	Interrupt line

2.11.21 Interrupt Pin Register (CFGIntPin) (Region: Configuration, Index: 0x3D, Access: R, Default: 0x01)

The interrupt pin register specifies which line the TVP4010 uses. The TVP4010 uses interrupt terminal INTAN.

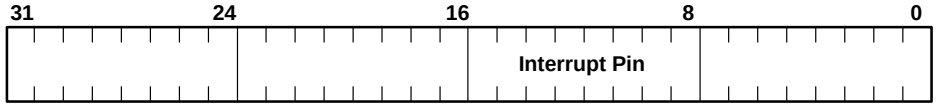


Table 2–25. Interrupt Pin Register

NAME	DESCRIPTION
Bits 8–15	Interrupt pin. TVP4010 uses interrupt terminal INTAN.

2.11.22 Minimum Grant Register (CFGMinGrant) (Region: Configuration, Index: 0x3E, Access: R, Default: Configuration Data)

The minimum grant register specifies how long of a burst period a PCI device needs.

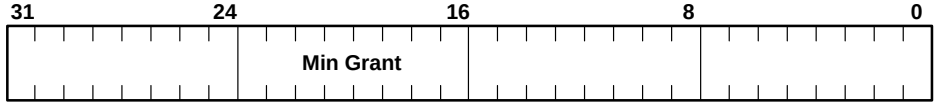


Table 2–26. Minimum Grant Register

NAME	DESCRIPTION
Bits 16–23	Minimum grant. Possible values are 00h, 40h, 80h, and C0h.

2.11.23 Maximum Latency Register (CFGMaxLat) (Region: Configuration, Index: 0x3F, Access: R, Default: Configuration Data)

The maximum latency register specifies how often the PCI device needs to gain access to the PCI bus. The possible values are 00h, 40h, 80h, and C0h.

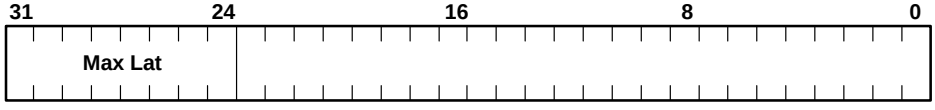


Table 2–27. Maximum Latency Register

NAME	DESCRIPTION
Bits 24–31	Maximum latency. Possible values are 00h, 40h, 80h, and C0h.

2.12 Region 0 Registers

2.12.1 Region 0 Address Map

The TVP4010 region zero is a 128-Kbyte region containing the control registers and the ports to and from the graphics processor. The control space is mapped in twice within the 128-Kbyte region. In the second 64K, the registers are mapped to be byte swapped for big-endian hosts.

Table 2–28. Region 0 Address Map

ADDRESS RANGE	REGION SELECT	BYTE SWAP
00000000 – 000007FF	Control status	No
00000800 – 00000FFF	Reserved (delta)	No
00001000 – 00001FFF	Memory control	No
00002000 – 00002FFF	GP FIFO access	No
00003000 – 00003FFF	Video control	No
00004000 – 00004FFF	RAMDAC	No
00005000 – 00005FFF	Auxiliary	No
00006000 – 00006FFF	VGA control	No
00007000 – 00007FFF	Reserved	No
00008000 – 0000FFFF	GP registers	No
00010000 – 000107FF	Control status	Yes
00010800 – 00010FFF	Reserved (delta)	Yes
00011000 – 00011FFF	Memory control	Yes
00012000 – 00012FFF	GP FIFO access	Yes
00013000 – 00013FFF	Video control	Yes
00014000 – 00014FFF	RAMDAC	Yes
00015000 – 00015FFF	Auxiliary	Yes
00016000 – 00016FFF	VGA control	Yes
00017000 – 00017FFF	Reserved	Yes
00018000 – 0001FFFF	GP registers	Yes

2.13 Control Status Registers

2.13.1 Reset Status Register (ResetStatus) (Region: Zero, Index: 0x00000000, Access: R/W, Default: 0x00000000)

Writing to the reset status register forces a software reset of the TVP4010 3D graphics processor. The software reset does not reset the PCI interface but is otherwise the same as a hardware reset.

The software reset takes a number of cycles and the graphics processor must not be used during the reset. A flag in the register is provided which indicates when a software reset is in progress.

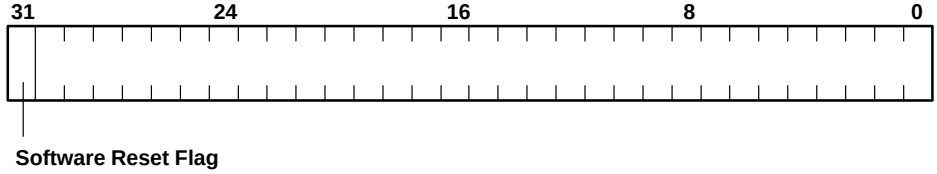


Table 2–29. Reset Status Register

NAME	DESCRIPTION	DESCRIPTION
Bits 0–30	Reserved	
Bit 31	Software reset flag	0 = The GC is ready for use
		1 = The GC is being reset and must not be used

2.13.2 Interrupt Enable Register (IntEnable) (Region: Zero, Index: 0x00000008, Access: R/W, Default: 0x00000000)

The interrupt enable register allows for a number of TVP4010 flags to generate a PCI interrupt. Five interrupt sources are defined below. At reset, all interrupt sources are disabled.

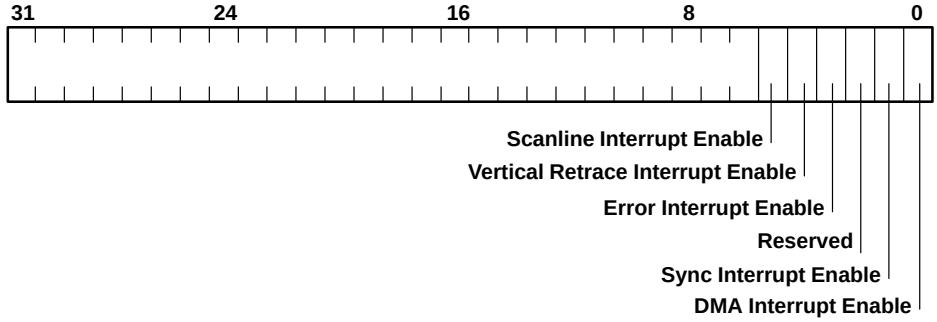


Table 2–30. Interrupt Enable Register

NAME	DESCRIPTION	
Bit 0	DMA interrupt enable	0 = Disable interrupt
		1 = Enable interrupt
Bit 1	Sync interrupt enable	0 = Disable interrupt
		1 = Enable interrupt
Bit 2	Reserved. Read as zero.	
Bit 3	Error interrupt enable	0 = Disable interrupt
		1 = Enable interrupt
Bit 4	Vertical retrace interrupt enable	0 = Disable interrupt
		1 = Enable interrupt
Bit 5	Scanline interrupt enable	0 = Disable interrupt
		1 = Enable interrupt
Bits 6–36	Reserved. Read as zero.	

2.13.3 Interrupt Flags Register (IntFlags) (Region: Zero, Index: 0x00000010, Access: R/W, Default: 0x00000000)

The interrupt flags register shows which interrupts are outstanding. Flag bits are reset by writing to this register with the corresponding bit set to a one. Flags at positions where the bits are set to zero will be unaffected by the write. (The exception is bit 31, which is read-only and reflects the state of the interrupt line from the VGA Unit. The VGA interrupt must be enabled and reset by accessing the VGA unit directly, but is visible in this register for convenience.)

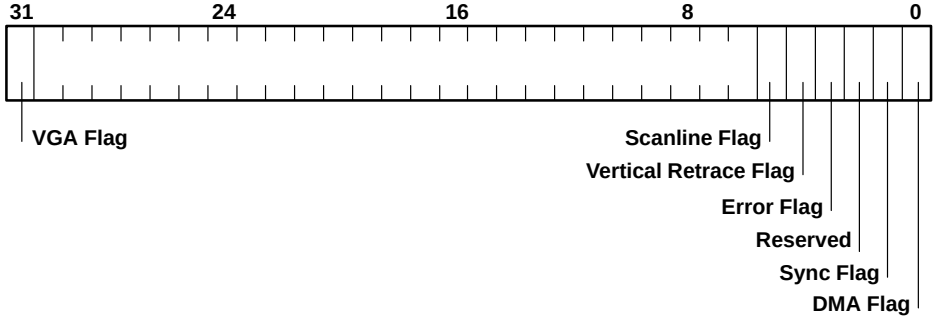


Table 2–31. Interrupt Flags Register

NAME	DESCRIPTION	
Bit 0	DMA flag	0 = No interrupt
		1 = Interrupt outstanding
Bit 1	Sync flag	0 = No interrupt
		1 = Interrupt outstanding
Bit 2	Reserved. Read as zero.	
Bit 3	Error flag	0 = No interrupt
		1 = Interrupt outstanding
Bit 4	Vertical retrace flag	0 = No interrupt
		1 = Interrupt outstanding
Bit 5	Scanline flag	0 = No interrupt
		1 = Interrupt outstanding
Bis 6–30	Reserved. Read as zero.	
Bit 31	VGA flag	0 = No interrupt
		1 = Interrupt outstanding

2.13.4 Input FIFO Space Register (InFIFOSpace) (Region: Zero, Index: 0x00000018, Access: R/W, Default: 0x00000020)

The input FIFO space register indicates the number of words that can currently be written to the input FIFO. This register can be read at any time and used to allow the controlling software to efficiently send data to the TVP4010 . If the DMA controller for the FIFO is in use, the value read is a snapshot of the current FIFO status.

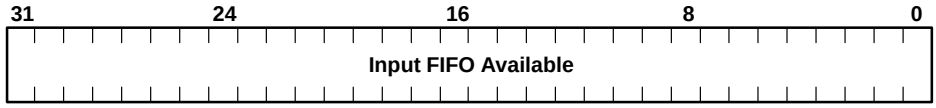


Table 2–32. Input FIFO Space Register

NAME	DESCRIPTION	
Bits 0–31	Input FIFO space. The number of empty words in the input FIFO. This number can be written before checking again for FIFO space availability.	Valid range: 0–32

2.13.5 Output FIFO Words Register (OutFIFOWords) (Region: Zero, Index: 0x00000020, Access: R, Default: 0x00000000)

The output FIFO words register indicates the number of words currently in the output FIFO. This register can be read at any time and used to allow the controlling software to efficiently read output data from the TVP4010.

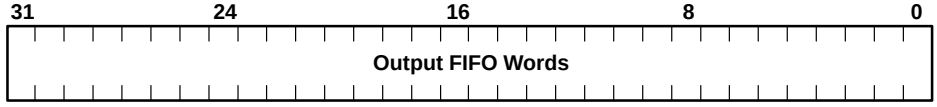


Table 2–33. Output FIFO Words Register

NAME	DESCRIPTION	
Bits 0–31	Output FIFO words. The number of valid words in the output FIFO. This number of words can be written before checking for more words.	Valid range: 0–8

2.13.6 DMA Start Address Register (DMAAdress) (Region: Zero, Index: 0x00000028, Access: R/W, Default: 0x00000000)

The DMA start address register should be loaded with the first PCI address for the buffer to be transferred to the GC when using the DMA controller.

Writing to the DMA count register loads the address into the DMA counter. Once a DMA has been set off, the next DMA start address may be loaded. A read of this register returns the last start value loaded even if a DMA is underway.

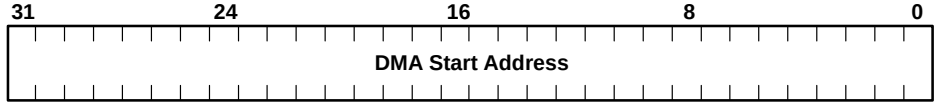


Table 2–34. DMA Start Address Register

NAME	DESCRIPTION
Bits 0–31	DMA start address. PCI start address for PCI master read transfer to the graphics core.

2.13.7 DMA Count Register (DMACount) (Region: Zero, Index: 0x00000030, Access: R/W, Default: 0x00000000)

The DMA count register should be loaded with the number of words to be transferred in a DMA operation. The action of loading a word count greater than zero sets off the DMA operation. The value read back from this register indicates the current number of words left to be transferred. This register should only be written to if the count is zero. It can be read at any time.

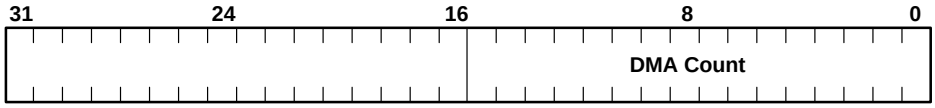


Table 2–35. DMA Count Register

NAME	DESCRIPTION	
Bits 0–15	DMA count. Number of words to be transferred in DMA operation. Undefined action if this register is written to when it is not zero.	Valid range: 0 to 65535

2.13.8 Error Flags Register (ErrorFlags) (Region: Zero, Index: 0x00000038, Access: R/W, Default: 0x00000000)

The error flags register shows which errors are outstanding on the TVP4010.

Flag bits are reset by writing to this register with the corresponding bit set to a 1. Flags at positions where the bits are set to 0 will be unaffected by a write.

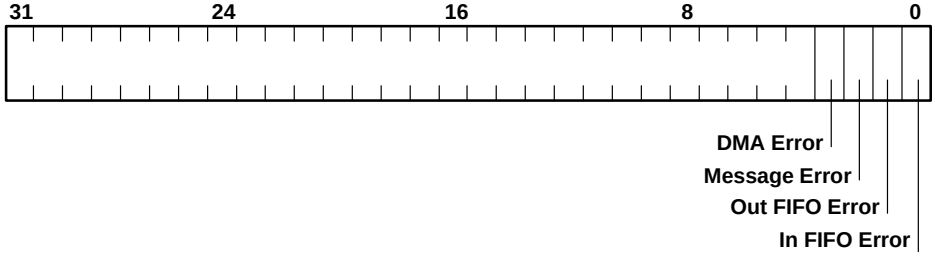


Table 2–36. Error Flags Register

NAME	DESCRIPTION	
Bit 0	Input FIFO error flag. Flag set on write to full input FIFO.	0 = No error
		1 = Error outstanding
Bit 1	Output FIFO error flag. Flag set on read from empty output FIFO.	0 = No error
		1 = Error outstanding
Bit 2	Message error flag. Flag set on incorrect mixing of access to the input FIFO space and the GC register space.	0 = No error
		1 = Error outstanding
Bit 3	DMA error flag. Flag set for direct or register access to input FIFO while DMA is in progress.	0 = No error
		1 = Error outstanding

2.13.9 Video Clock Control Register (Register VClkCtl) (Region: Zero, Index: 0x00000040, Access: R/W, Default: 0x00000000)

The bottom two bits of the video clock control register drive two physical output terminals on the TVP4010. These terminals can be used to program an external video clock PLL chip. Some RAMDAC devices require a minimum period between accesses, and an eight-bit field is provided in this register to program the number of PCI clocks to be counted between each RAMDAC access. A further bit is used to indicate whether auxiliary bus I/O accesses are little-endian or big-endian.

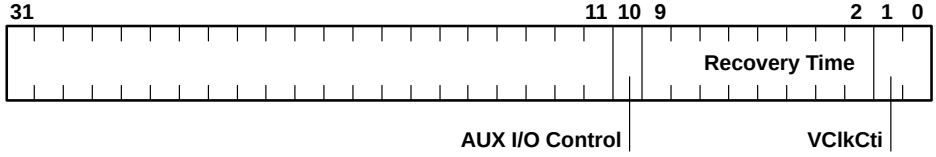
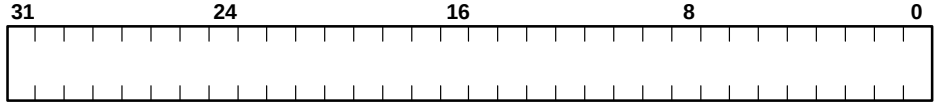


Table 2–37. Video Clock Control Register

NAME	DESCRIPTION	
Bit 0	VidCtl (0) terminal	
Bit 1	VidCtl (1) terminal	
Bits 2–9	Recovery time. Number of PCI clocks to count between RAMDAC accesses.	
Bit 10	AUX I/O control.	0 = Treat PCI I/O space accesses to auxiliary bus as little-endian.
		1 = Treat PCI I/O space accesses to auxiliary bus as big-endian.
Bits 11–32	Reserved. Read as zero.	

2.13.10 Test Register (TestRegister) (Region: Zero, Index: 0x00000048, Access: R/W, Default: 0x00000000)

Writes to the test register have an undefined effect.



2.13.11 Aperture 1 Control Register (ApertureOne)
(Region: Zero, Index: 0x00000050, Access: R/W, Default: 0x00000000)

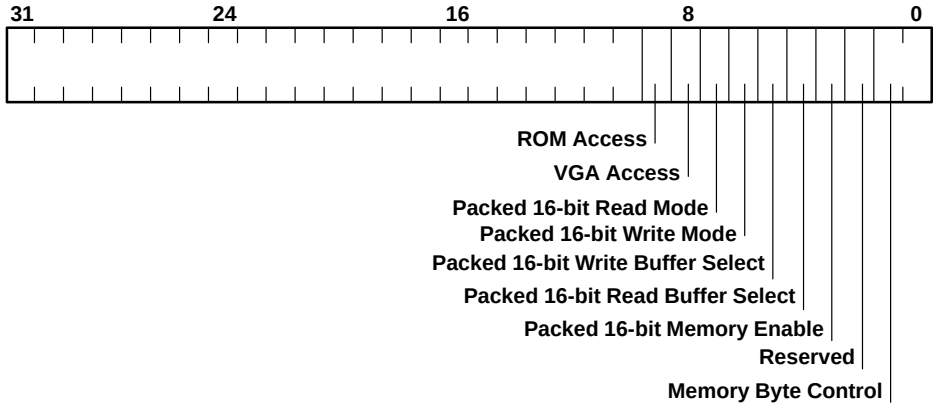


Table 2–38. Aperture 1 Control Register

NAME	DESCRIPTION	
Bits 0–1	Memory byte control	0 = Standard
		1 = Byte swapped
		2 = Half word swapped
		3 = Reserved
Bit 2	Reserved (read only)	
Bit 3	Packed 16-bit (1:5:5:5) memory enable	0 = Disable packed 16-bit mode
		1 = Enable packed 16-bit mode
Bit 4	Packed 16-bit read buffer select	0 = Selected buffer A for read access
		1 = Selected buffer B for read access
Bit 5	Packed 16-bit write buffer select	0 = Selected buffer A for write access
		1 = Selected buffer B for write access
Bit 6	Packed 16-bit write mode	0 = Disable double writes
		1 = Enable double writes
Bit 7	Packed 16-bit ready mode	0 = Read buffer selected by bit 4 of this register
		1 = Read buffer selected by memory contents (bit 31)
Bit 8	VGA access	0 = Address memory controller directly
		1 = Address memory through VGA subsystem
Bit 9	ROM access	0 = Use this aperture to access memory (VGA or direct)
Bit 9	ROM access	1 = Use this aperture to access the expansion ROM
Bits 10–31	Reserved (all bits zero) (read only)	

2.13.12 Aperture 2 Control Register (ApertureTwo) (Region: Zero, Index: 0x00000058, Access: R/W, Default: 0x00000000)

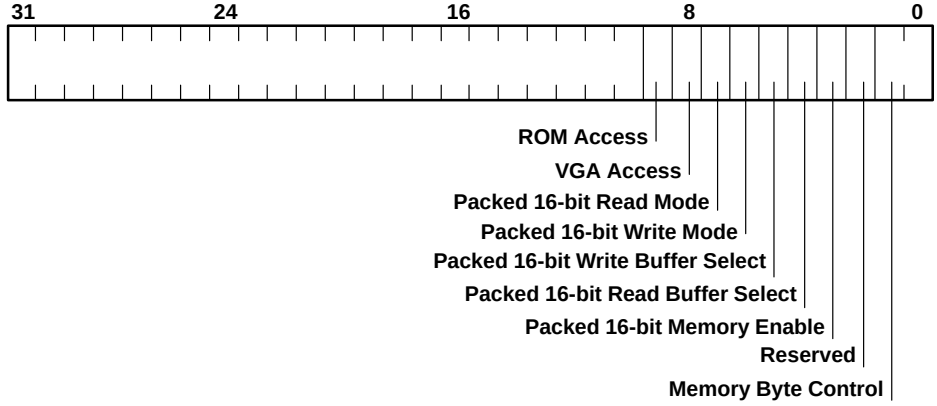


Table 2–39. Aperture 2 Control Register

NAME	DESCRIPTION	
Bits 0–1	Memory byte control	0 = Standard
		1 = Byte swapped
		2 = Half word swapped
		3 = Reserved
Bit 2	Reserved (read only)	
Bit 3	Packed 16-bit (1:5:5:5) memory enable	0 = Disable packed 16-bit mode
		1 = Enable packed 16-bit mode
Bit 4	Packed 16-bit read buffer select	0 = Selected buffer A for read access
		1 = Selected buffer B for read access
Bit 5	Packed 16-bit write buffer select	0 = Selected buffer A for write access
		1 = Selected buffer B for write access
Bit 6	Packed 16-bit write mode	0 = Disable double writes
		1 = Enable double writes
Bit 7	Packed 16-bit readv mode	0 = Read buffer selected by bit 4 of this register
		1 = Read buffer selected by memory contents (bit 31)
Bit 8	VGA access	0 = Address memory controller directly
		1 = Address memory through VGA subsystem
Bit 9	ROM access	0 = Use this aperture to access memory (VGA or direct)
		1 = Use this aperture to access the expansion ROM
Bits 10–31	Reserved (all bits zero) (read only)	

2.13.13 DMA Control Register (DMAControl) (Region: Zero, Index: 0x00000058, Access: R/W, Default: 0x00000000)

The DMA control register sets up the data transfer modes for the DMA controller. The DMA controller can be set to little-endian or big-endian (byte swapped).

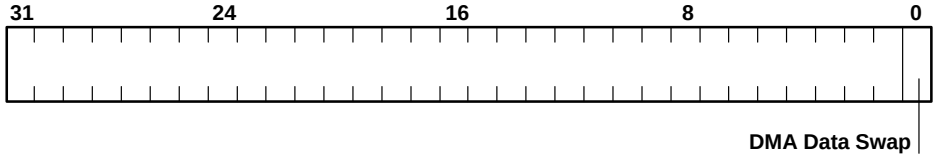


Table 2–40. DMA Control Register

NAME	DESCRIPTION	DESCRIPTION
Bit 0	DMA byte swap control	0 = Little endian
		1 = Big endian

2.13.14 FIFO Disconnect Register (FIFODiscon) (Region: Zero, Index: 0x00000068, Access: R/W, Default: 0x00000000)

The FIFO disconnect register enables the input and output FIFO disconnect signals which drive two physical terminals on the TVP4010. Disconnects are disabled at reset.

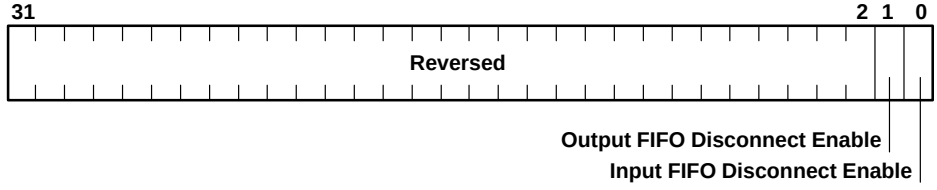


Table 2–41. FIFO Disconnect Register

NAME	DESCRIPTION	DESCRIPTION
Bit 0	Input FIFO disconnect enable	0 = Disable
		1 = Enable
Bit 1	Output FIFO disconnect	0 = Disable
		1 = Enable
Bits 2–31	Reserved, read as zero (read only)	

2.13.15 Chip Configuration Register (ChipConfig) (Region: Zero, Index: 0x00000070, Access: R/W, Default: Configuration Data)

Most of the sampled values from the configuration terminals are loaded into the chip configuration register on the trailing edge of reset. This register can then be read back over the PCI bus to allow the host to determine how the TVP4010 has been configured and to modify fields of the configuration if required.

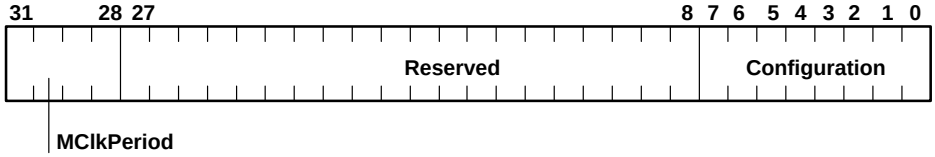


Table 2–42. Chip Configuration Register

NAME	DESCRIPTION	
Bit 0	BaseClassZero	0 = Use the correct PCI base class code
		1 = Force PCI base class code to be zero
Bit 1	VGAEnable	0 = Disable internal VGA subsystem
		1 = Enable internal VGA subsystem
Bit 2	VGAFixed	0 = Disable VGA fixed address decoding
		1 = Enable VGA fixed address decoding
Bit 3	AuxEnable	0 = External auxiliary device not present
		1 = External auxiliary device is present
Bit 4	AuxIOEnable	0 = Disable Aux I/O base address register
		1 = Enable Aux I/O base address register
Bit 5	RetryDisable	0 = Enable PCI retry using disconnect-without-data
		1 = Disable PCI retry using disconnect-without-data
Bit 6	DeltaEnable	0 = External delta device not present
		1 = External delta device is present
Bit 7	ShortReset	0 = Generate normal reset
		1 = Generate short reset
Bits 8–27	Reserved, read as zero (read only)	
Bits 28–31	MClkPeriod (read only). Value given in ns starting from 10 ns: 0000 = 10 ns MCLK period (100 MHz). 1111 = 25 ns MCLK period (40 MHz).	

2.14 Memory Control Registers

Refer to the memory system section for details on programming the memory control registers.

2.14.1 Reboot Register (Reboot) (Region: Zero, Index: 0x1000, Access: W, Default: Configuration Data)

Writing to the reboot register instructs the memory controller to reboot the SGRAMs. This involves going through the reset sequence and loading the boot address register. A reboot does not reload the configuration data; registers maintain their contents until a reset. A read from this register returns zero.

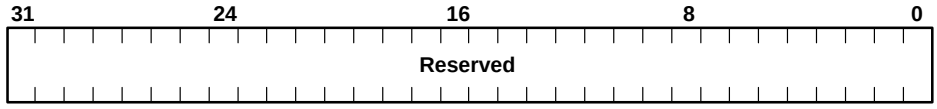


Table 2–43. Reboot Register

NAME	DESCRIPTION
Bits 0–31	Reserved, read as zero (read only)

2.14.2 ROM Control Register (RomControl) (Region: Zero, Index: 0x1040, Access: R/W, Default: Configuration Data)

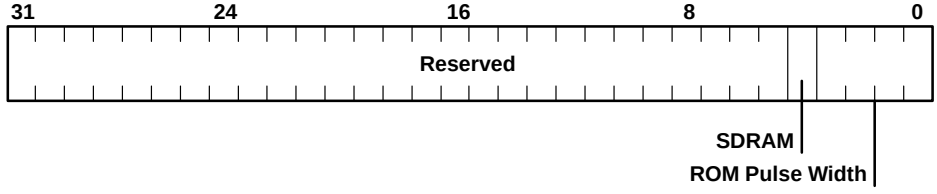


Table 2–44. ROM Control Register

NAME	DESCRIPTION	
Bits 0–3	ROM Pulse Width, TimeRPW	
Bit 4	SDRAM	0 = SGRAM fitted
		1 = SDRAM fitted
Bits 5–31	Reserved, read as zero	

2.14.3 Boot Address Register (BootAddress) (Region: Zero, Index: 0x1080, Access: R/W, Default: Configuration Data)

The value in the boot address register specifies the contents of the SGRAM mode register at boot time. Boot time is either at chip reset or when a reboot is caused by writing to a register.

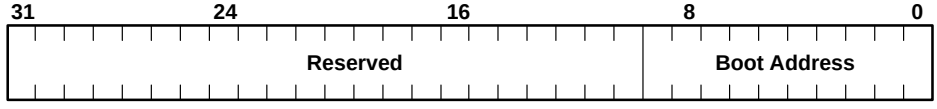


Table 2–45. Boot Address Register

NAME	DESCRIPTION
Bits 0–9	Boot address. See memory data sheet for bit pattern.
Bits 10–31	Reserved, read as zero

2.14.4 Memory Configuration Register (MemConfig) (Region: Zero, Index: 0x10C0, Access: R/W, Default: Configuration Data)

The memory configuration register holds configuration data for the memory controller. If it is written to, there is an automatic reboot of the memory. The correct sequence is to load the boot address, then change this register to match the boot address.

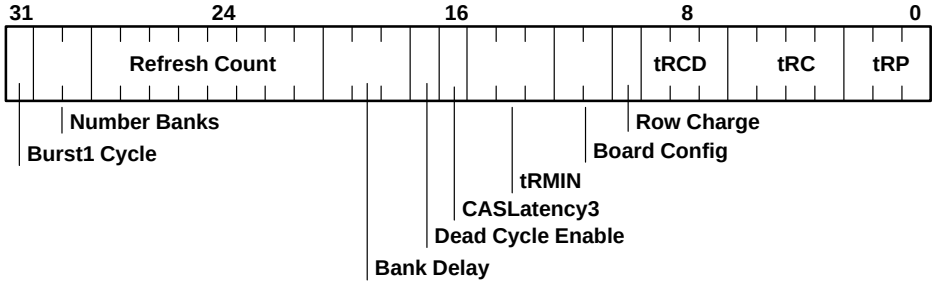


Table 2–46. Memory Configuration Register

NAME	DESCRIPTION	
Bits 0–2	TimeRP. Number of MCLKs from issuing PRECHARGE to issuing an ACTIVATE command. Should be set to tRP – 1.	
Bits 3–6	TimeRC. Number of MCLKs from issuing AUTO-REFRESH to issuing another command. Should be set to tRC – 2.	
Bits 7–9	TimeRCD. Number of MCLKs from issuing RAS to issuing CAS. Should be set to tRCD – 2.	
Bit 10	RowCharge	0 = Row charge disabled
		1 = Row charge enabled
Bits 11–12	BoardConfig. Value of configuration resistors, not used by memory controller.	
Bits 13–15	TimeRASMin. Number of active clocks for the minimum row active time. Should be set to tRAS – 3 unless this results in a value of zero.	
Bit 16	CASLatency3	0 = CAS latency of 2
		1 = CAS latency of 3
Bit 17	DeadCycleEnable	0 = Do not insert dead cycle between reads and writes.
		1 = Insert dead cycle between reads and writes.
Bits 18–20	BankDelay. Defines read burst length. Should be set to burst length – 1.	
Bits 21–28	RefreshCount. Defines period between AUTO-REFRESH commands. The count is in MCLKs/16.	
Bits 29–30	NumberBanks	0 = 1 bank (2 Mbytes)
		1 = 2 banks (4 Mbytes)
		2 = 3 banks (6 Mbytes)
		3 = 4 banks (8 Mbytes)
Bit 31	Burst1Cycle	0 = Do not assume burst length of 1
		1 = Assume burst length of 1

2.14.5 Bypass Write Mask Register (BypassWriteMask) (Region: Zero, Index: 0x1100, Access: R/W, Default: Undefined)

The bypass write mask register contains the mask used to protect bits from modification by bypass writes to memory.

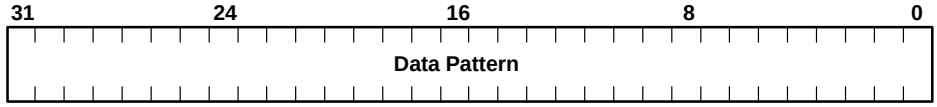


Table 2–47. Bypass Write Mask Register

NAME	DESCRIPTION	
Bits 0–31	Data pattern	0 = Corresponding bit in memory protected
		1 = Corresponding bit in memory writable

2.14.6 Framebuffer Write Mask Register (FramebufferWriteMask) (Region: Zero, Index: 0x1140, Access: R, Default: Undefined)

The framebuffer write mask register contains the mask used to protect bits from modification by framebuffer writes to memory. It can be read from the bypass, but can only be modified through the framebuffer write unit in the graphics core.

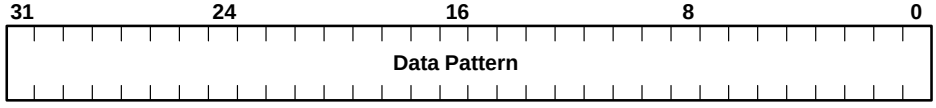


Table 2–48. Framebuffer Write Mask Register

NAME	DESCRIPTION	
Bits 0–31	Data pattern	0 = Corresponding bit in memory protected
		1 = Corresponding bit in memory writable

2.14.7 Count Register (Count) (Region: Zero, Index: 0x1180, Access: R, Default: Undefined)

The count register contains a free running count that may be used for any purpose. The counter is driven by MCLK and wraps to zero at overflow.

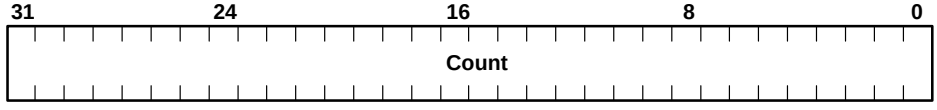


Table 2–49. Count Register

NAME	DESCRIPTION
Bits 0–31	Count

2.15 Video Control Registers

Refer to the video unit section for details on programming the video control registers.

2.15.1 Screen Base Register (ScreenBase) (Region: Zero, Index: 0x3000, Access: R/W, Default: Undefined)

The screen base register contains the address of the pixel in the top left of the screen. The value of this register is ignored until vertical blank. When it is loaded, the BypassPending bit is set in the video control register until it is used.

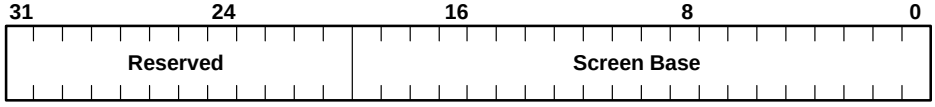


Table 2–50. Screen Base Register

NAME	DESCRIPTION
Bits 0–19	ScreenBase. Base address of screen in 64-bit units.
Bits 20–31	Reserved (read only)

2.15.2 Screen Stride Register (ScreenStride) (Region: Zero, Index: 0x3008, Access: R/W, Default: Undefined)

The screen stride register contains the stride between the scan lines of the display.

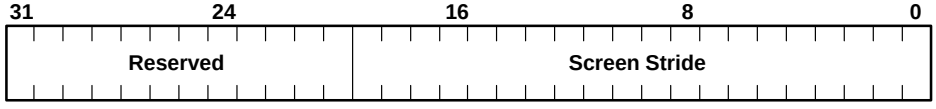


Table 2–51. Screen Stride Register

NAME	DESCRIPTION
Bits 0–19	ScreenStride between scanlines in 64-bit units.
Bits 20–31	Reserved, read as zero

2.15.3 Horizontal Total Register (HTotal) (Region: Zero, Index: 0x3010, Access: R/W, Default: Undefined)

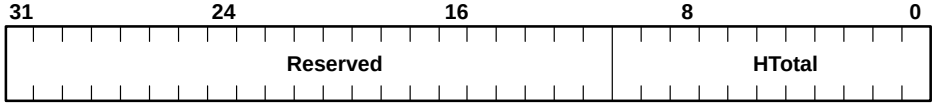


Table 2–52. Horizontal Total Register

NAME	DESCRIPTION
Bits 0–10	HTotal. Last 32-bit unit, including HBlank, on screen (i.e. horizontal total value – 1).
Bits 11–31	Reserved, read as zero

2.15.4 Horizontal Gate End Register (HgEnd) (Region: Zero, Index: 0x3018, Access: R/W, Default: Undefined)

The horizontal gate end register contains the end of the gate period. The gate period defines the period during which video data is not clocked from the TVP4010. The value of this register is not used until vertical blank.

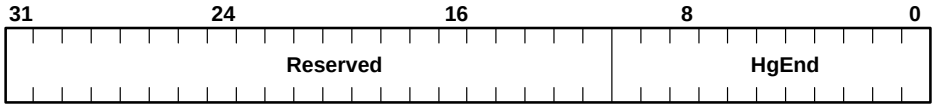


Table 2–53. Horizontal Gate End Register

NAME	DESCRIPTION
Bits 0–10	HgEnd. Last 32-bit unit in gate period (i.e. gate period-1).
Bits 11–31	Reserved, read as zero

2.15.5 Horizontal Blank End Register (HbEnd) (Region: Zero, Index: 0x3020, Access: R/W, Default: Undefined)

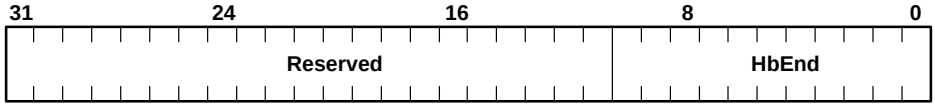


Table 2–54. Horizontal Blank End Register

NAME	DESCRIPTION
Bits 0–10	HbEnd. Last 32-bit unit in horizontal blank period (i.e. blank period-1).
Bits 11–31	Reserved, read as zero

2.15.6 Horizontal Sync Start Register (HsStart) (Region: Zero, Index: 0x3028, Access: R/W, Default: Undefined)

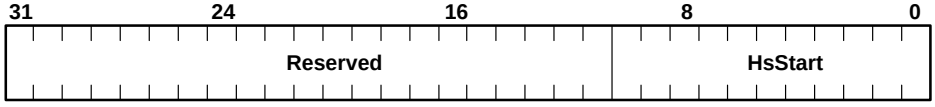


Table 2–55. Horizontal Sync Start Register

NAME	DESCRIPTION
Bits 0–10	HsStart. First 32-bit unit in horizontal sync period (i.e. front porch period).
Bits 11–31	Reserved, read as zero

2.15.7 Horizontal Sync End Register (HsEnd) (Region: Zero, Index: 0x3030, Access: R/W, Default: Undefined)

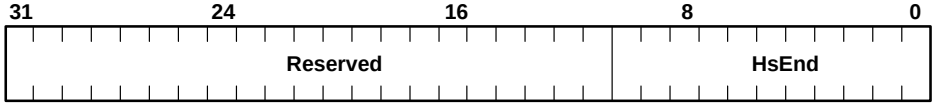


Table 2–56. Horizontal Sync End Register

NAME	DESCRIPTION
Bits 0–10	HsEnd. First 32-bit unit out of horizontal sync period (i.e. front porch period + sync width).
Bits 11–31	Reserved, read as zero

2.15.8 Vertical Total Register (VTotal) (Region: Zero, Index: 0x3038, Access: R/W, Default: Undefined)

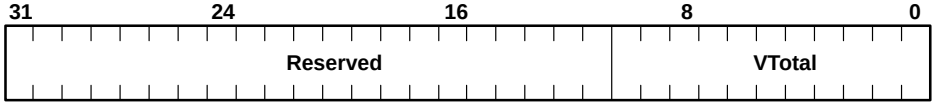


Table 2–57. Vertical Total Register

NAME	DESCRIPTION
Bits 0–10	VTotal. Last scanline on screen, including vertical blank (i.e. number of lines -1).
Bits 11–31	Reserved, read as zero

2.15.9 Vertical Blank End Register (VbEnd) (Region: Zero, Index: 0x3040, Access: R/W, Default: Undefined)

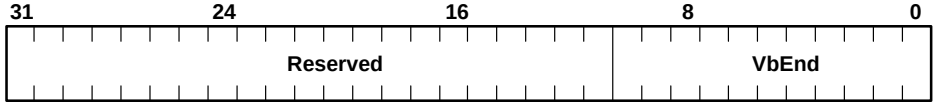


Table 2–58. Vertical Blank End Register

NAME	DESCRIPTION
Bits 0–10	VbEnd. First scanline out of vertical blank (i.e. blank period).
Bits 11–31	Reserved, read as zero

2.15.10 Vertical Sync Start Register (VsStart) (Region: Zero, Index: 0x3048, Access: R/W, Default: Undefined)

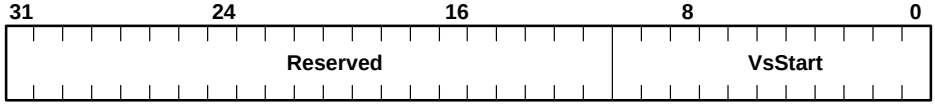


Table 2–59. Vertical Sync Start Register

NAME	DESCRIPTION
Bits 0–10	VsStart. Scanline before start of vertical sync (i.e. period of front porch -1).
Bits 11–31	Reserved, read as zero

2.15.11 Vertical Sync End Register (VsEnd) (Region: Zero, Index: 0x3050, Access: R/W, Default: Undefined)

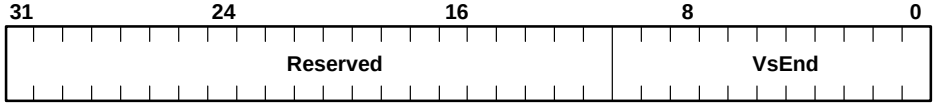


Table 2–60. Vertical Sync End Register

NAME	DESCRIPTION
Bits 0–10	VsEnd. Last scanline in vertical sync (i.e. period of front porch + sync width -1).
Bits 11–31	Reserved, read as zero

2.15.12 Video Control Register (VideoControl) (Region: Zero, Index: 0x3058, Access: R/W, Default: 0x0)

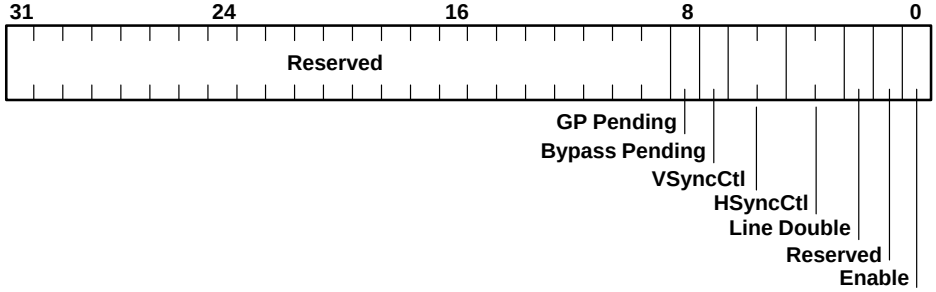


Table 2–61. Video Control Register

NAME	DESCRIPTION	
Bit 0	Enable	0 = GP video disabled
		1 = GP video enabled
Bit 1	Reserved, read as zero	
Bit 2	LineDouble	0 = Line doubling disabled
		1 = Line doubling enabled. If enabled, each scanline is displayed twice to increase the effective frequency of low resolution screens.
BitS 3-4	HSyncCtL	0 = Forced high
		1= Active high
		2 = Forced low
		3 = Active low
Bits 5–6	VSyncCtl	0 = Forced high
		1 = Active high
		2 = Forced low
		3 = Active low
Bit 7	BypassPending	0 = Screenbase value used
		1 = New screenbase value waiting to be used. Read only bit, set when Screenbase is loaded through the bypass.
Bit 8	GPPending	0 = Screenbase value used
		1 = New screenbase value waiting to be used. Read only bit, set when screenbase is loaded through the graphics processor.
Bits 9–31	Reserved, read as zero	

2.15.13 Interrupt Line Register (InterruptLine) (Region: Zero, Index: 0x3060, Access: R/W, Default: Undefined)

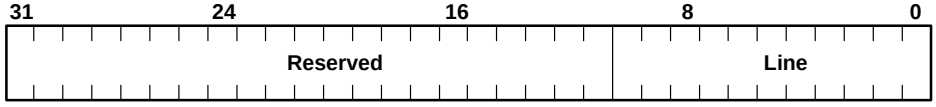


Table 2–62. Interrupt Line Register

NAME	DESCRIPTION
Bits 0–10	Line. Generate interrupt at start of this line.
Bits 11–31	Reserved, read as zero

2.15.14 Display Data Channel Data Register (DDCData) (Region: Zero, Index: 0x3068, Access: R, Default: Undefined)

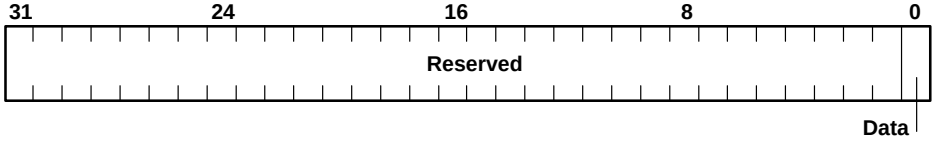


Table 2–63. Display Data Channel Data Register

NAME	DESCRIPTION
Bits 0	Data. Data read from DCC terminal
Bits 1–11	Reserved, read as zero

2.15.15 Line Count Register (LineCount) (Region: Zero, Index: 0x3070, Access: R/W, Default: Undefined)

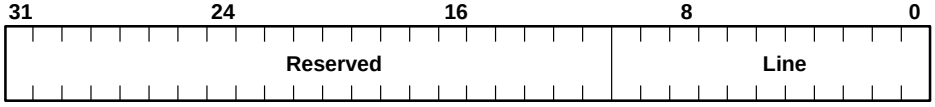


Table 2–64. Line Count Register

NAME	DESCRIPTION
Bits 0–10	Line. Current line.
Bits 11–31	Reserved, read as zero

2.16 VGA Interface

In addition to the standard VGA registers, the TVP4010 supports two extended registers, the VGA control register and the mode 640 register.

2.16.1 VGA Memory

The VGA memory is accessed through the VGA legacy memory addresses. The VGA memory can also be accessed through the TVP4010 memory apertures by setting the VGA access bit in either the aperture one or aperture two register. The memory address for the VGA is formed from bits 16 down to 2 of the incoming bus address. This results in the 128 Kbyte VGA memory space being aliased within the 8 Mbyte total region size. No byte swapping or other data formatting is performed when accessing the VGA memory in this manner.

2.16.2 VGA Registers

The TVP4010 standard VGA registers are accessed through the VGA legacy IO addresses. These registers are also mapped into a 4-Kbyte space at offset 0x6000h in region 0. The address for the VGA unit is formed from bits 9 down to 2 of the incoming bus address. So, for example, VGA register 0x3C4h can be addressed at offsets 0x63C4h, 0x67C4h, 0x6BC4h, and 0x6FC4h.

2.16.3 VGA Control Register (VGAControlReg) (Region: Zero, Index: , Access: R/W, Default: 0x0B)

This extended VGA register is accessed as index 5 through the sequencer index register at port 0x3C4h. Data is written to port 3C5h.

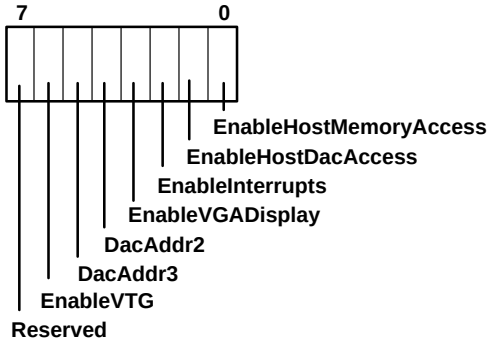


Table 2–65. VGA Control Register

NAME	DESCRIPTION	
Bit 0	EnableHostMemoryAccess	0 = Disable host accesses to memory
		1 = Enable host accesses to memory
Bit 1	EnableHostDacAccess	0 = Disable host accesses to RAMDAC
		1 = Enable host accesses to RAMDAC
Bit 2	EnableInterrupts	0 = Disable interrupts from VGA
		1 = Enable interrupts from VGA
Bit 3	EnableVGADisplay	0 = Disable VGA display, enable graphics processor display.
		1 = Enable VGA display, disable graphics processor display.
Bit 4	DacAddr2. Sets bit 2 of RAMDAC address.	
Bit 5	DacAddr3. Sets bit 3 of RAMDAC address.	
Bit 6	EnableVTG	0 = Stops VTG running and producing sync pulses
		1 = Enables VTG to produce sync pulses. Only has effect when EnableVGADisplay has been set to zero.
Bit 7	Reserved. Read as zero.	

2.16.4 Mode 640 Register (Mode64Reg) (Region: Zero, Index: , Access: R/W, Default: 0x0B)

The mode 640 register is an extended VGA register that is accessed as index 9 through the graphics index register at port 3CEh. Data is written to port 3CFh.

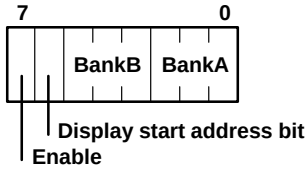


Table 2–66. Mode 640 Register

NAME	DESCRIPTION	
Bits 0–2	BankA. Additional address bits for accesses between A0000h and B0000h.	
Bits 3–5	BankB. Additional address bits for accesses between B0000h and C0000h.	
Bit 6	Bit 16 of display start address. Read as zero.	
Bit 7	Enable	0 = Mode640 disabled
		0 = Mode640 disabled

2.17 Memory System

The TVP4010 memory system is intended for use with SGRAM or SDRAM memory devices. A typical organization is shown in Figure 2–2.

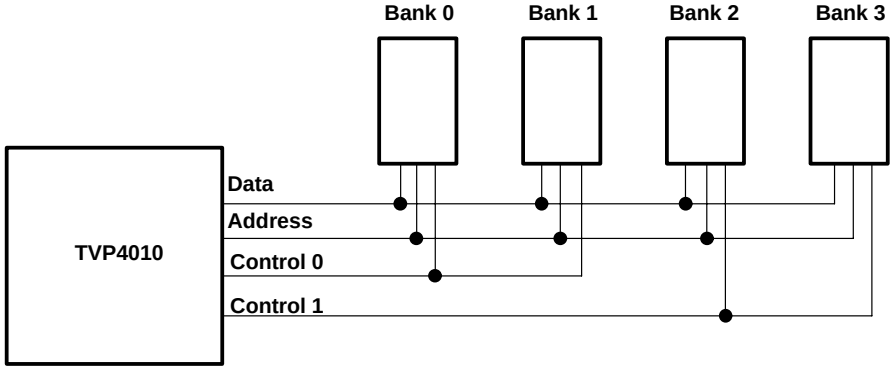


Figure 2–2. Organization of Memory Devices

Each bank is made up of two 32-bit wide devices. The data and address lines are common to all the memory devices. There are two sets of control lines which are provided to reduce loading: they are driven identically. The example above shows one set of control lines driving bank 0 and bank 1, with the second set driving bank 2 and bank 3. This organization is preferable if the second two banks are on a mezzanine connector as it eases routing and termination of clock lines. Alternatively the control lines could be split along the upper and lower devices in each bank.

2.17.1 System Parameters

The various timing parameters used to control synchronous memories can be adjusted to allow for optimum performance depending on the memory speed grade and the TVP4010 system clock frequency (MCLK).

The following parameters are used to control accesses to memory. These values are usually set at reset from configuration resistors. Each field defines the operation of the memory controller, with the exception of the boot address field which is loaded directly into the memory device. It is very important that the boot address is consistent with the memory controller parameters, failing to do this may damage the memory devices. The reset configuration may be over-written following reset.

2.17.2 TimeRPW

This parameter defines, in MCLK cycles, the duration of the ROM control signals. The duration of the EPROM read pulse is TimeRPW + 1; the duration of the ROM write pulse is TimeRPW – 2.

2.17.3 RowCharge

This flag determines the method used to load the Special Mode Register in the SGRAM. If set high, the memory controller assumes that the Special Mode Register may be accessed when one internal bank is IDLE and the other is ROW-ACTIVE.

2.17.4 TimeRCD

This parameter defines, in MCLK cycles, the time from issuing a RAS to the SGRAM before CAS is active. This is usually referred to in the SGRAM data sheets as tRCD and will be assigned by the memory controller as TimeRCD + 2.

2.17.5 TimeRC

This parameter defines, in MCLK cycles, the time from issuing an AUTO–REFRESH command to the SGRAM being able to accept another command. This is usually referred to in the SGRAM data sheets as tRC and will be assigned by the memory controller as TimeRC + 2.

2.17.6 TimeRP

This parameter defines, in MCLK cycles, the time from issuing a PRECHARGE command to the SGRAM being able to accept an ACTIVATE command (RAS). This is usually referred to in the SGRAM data sheets as tRP, and will be assigned by the memory controller as TimeRP + 1.

2.17.7 CASLatency3

This flag determines the CAS latency expected by the memory controller. If set high the controller expects the SGRAM to be operating with a CAS latency of 3. If set low the controller expects a CAS latency of 2.

2.17.8 BootAddress

This parameter defines the value of the Mode Register loaded into the SGRAM at the end of the boot sequence (see data sheet). Items to note: Burst type should be sequential, burst length should be consistent with the Burst1Cycle flag and CAS latency should be consistent with the CAS3Latency flag. All other bits in the BootAddress field should be set low.

2.17.9 NumberBanks

This field defines the size of SGRAM array being used. Values are 00 = 2 Mbytes, 01 = 4 Mbytes, 10 = 6 Mbytes, 11 = 8 Mbytes.

2.17.10 RefreshCount

This parameter defines the period between AUTO–REFRESH commands being issued to the SGRAM. The count is in MCLKs/16 i.e. if RefreshCount = 1, the SGRAM will be refreshed every 16 MCLK cycles. For the required refresh rate, see the SGRAM data sheet.

2.17.11 TimeRASMin

This parameter defines, in MCLK cycles, the minimum row active time. This is sometimes referred to as the active-to-precharge period. It is assigned by the memory controller as tRAS (in MCLK cycles) + 3. However, loading the MemConfig register field or setting the configuration resistors to a value of 0 is invalid.

2.17.12 DeadCycleEnable

If this flag is set high the memory controller will insert a turnaround cycle when changing from a READ to a WRITE command. Some SGRAM speed grades may require this.

2.17.13 BankDelay

This parameter defines the READ burst length of the SGRAM being used. It should always be consistent with the BootAddress parameter and should be set to burst length – 1.

2.17.14 Burst1Cycle

This flag, if set high, allows the memory controller to assume a burst length of 1 for the SGRAM. It should always be consistent with the SGRAM BootAddress parameter.

2.17.15 SDRAM

If this flag is set high, the memory controller will assume that SDRAM is fitted as the memory array. It will disable all block fills and bit-masked writes. Any block fill operations will be ignored, any masked writes will be converted to non-masked writes.

2.18 Recommended Parameter Values

The following values are recommended for a TVP4010 system running with an MCLK of 50 MHz and using Samsung SGRAM (–12) parts. The total SGRAM size is 4 Mbytes.

Table 2–67. Parameter Values, MCLK = 50 MHz and 4 Mbytes

PARAMETER	VALUE
RowCharge	0
TimeRCD	000
TimeRC	0100
TimeRP	001
CAS3Latency	0
BootAddress	000010000
NumberBanks	01
RefreshCount	00110000
TimeRASMin	001
DeadCycle	0
BankDelay	000
Burst1Cycle	1
SDRAM	0

The following values are recommended for a TVP4010 system running with an MCLK of 66 MHz and using NEC SGRAM (-12) parts. The total SGRAM size is 6 Mbytes. The CAS3Latency flag is set high. This is due to the access time of the (-12) part relative to the bus speed. If a CAS latency of 2 was used, the part may not drive data onto the bus in time for the read cycle to complete.

Table 2–68. Parameter Values, MCLK = 66 MHz and 6 Mbytes

PARAMETER	VALUE
RowCharge	1
TimeRCD	001
TimeRC	0110
TimeRP	010
CAS3Latency	1
BootAddress	000110000
NumberBanks	10
RefreshCount	01000001
TimeRASMin	001
DeadCycle	1
BankDelay	000
Burst1Cycle	1
SDRAM	0

The following values are recommended for a TVP4010 system running with an MCLK of 66 MHz and using NEC SGRAM (-10) parts. The total SGRAM size is 8 Mbytes.

Table 2–69. Parameter Values, MCLK = 66 MHz and 8 Mbytes

PARAMETER	VALUE
RowCharge	1
TimeRCD	001
TimeRC	0110
TimeRP	001
CAS3Latency	0
BootAddress	000010000
NumberBanks	11
RefreshCount	01000001
TimeRASMin	001
DeadCycle	1
BankDelay	000
Burst1Cycle	1
SDRAM	0

2.19 Using the Video Unit

Figure 2–3 shows the parameters that are used to control the display of images generated by the graphics processor. Any images generated by the VGA unit are displayed by the VGA which should be programmed in accordance with normal VGA practice.

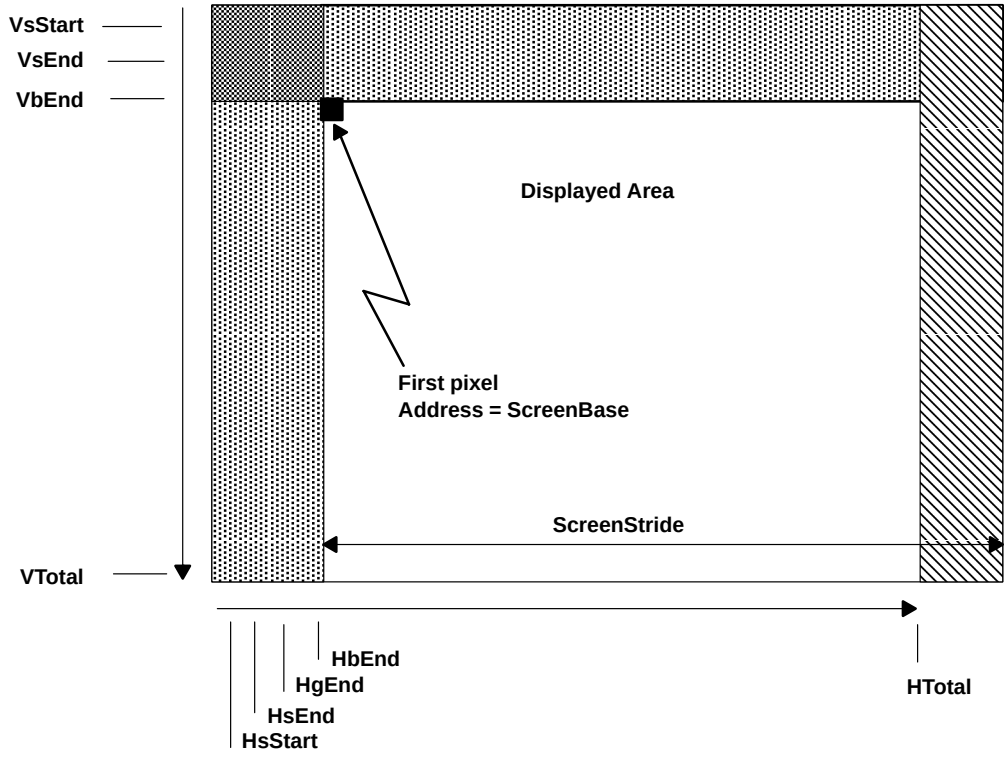


Figure 2–3. Video Timing Parameters

2.20 Example Timing Values

2.20.1 Timing Values for 640 x 480 16 BPP 75 Hz

Table 2–70. Timing Values for 640 x 480 16 BPP 75 Hz

PARAMETER	HEX	DECIMAL
HTotal	000001A3	419
HsStart	00000008	8
HsEnd	00000028	40
HbEnd	00000064	100
HgEnd	00000064	100
VTotal	000001F3	499
VsStart	00000000	0
VsEnd	00000003	3
VbEnd	00000014	20
ScreenStride	000000A0	160
ScreenBase	00000000	0
VideoControl	00000029	41

2.20.2 Timing Values for 800 x 600 32 BPP 75 Hz

Table 2–71. Timing Values for 800 x 600 32 BPP 75 Hz

PARAMETER	HEX	DECIMAL
HTotal	0000041F	1055
HsStart	00000010	16
HsEnd	00000060	96
HbEnd	00000100	256
HgEnd	00000100	256
VTotal	00000270	624
VsStart	00000000	0
VsEnd	00000003	3
VbEnd	00000019	25
ScreenStride	00000190	400
ScreenBase	00000000	0
VideoControl	00000029	41

2.21 Display Data Channel (DDC)

The DDC interface allows the TVP4010 to read timing information from a compatible monitor. The data is read one bit at a time, and is clocked from the monitor by the vertical sync signal. The vertical sync should be controlled directly from software using the video configuration register.

Vertical sync should be driven high and the data will become valid 30 microseconds later; when the data has been read the vertical sync should be driven low for at least 20 microseconds before it is driven high again. Accurate timing can be derived from the counter in the memory controller register group.

2.22 Auxiliary Bus

The auxiliary bus allows an additional slave device to be added to the TVP4010. It shares the same address and data lines as the RAMDAC processor interface, but has its own read, write, and wait signals. The bus is asynchronous, and the slave can insert wait states by driving the wait signal.

2.23 Reset Control

A number of parameters for the TVP4010 are initialized at reset time, such as memory size and speed. The reset state is configured with resistors connected to the memory and video port data terminals. The state of the data terminals is sampled at the end of reset. Various parameters may be configured.

- Memory size
- Memory RAS and CAS timings
- ROM timings

To set a bit to 1 the relevant data terminal should be tied to V_{CC} with a 4K7 resistor. To set a bit to 0 the relevant data terminal should be tied to ground with a 4K7 resistor. Refer to the section on the relevant unit for details on the meaning of the fields.

Table 2–72. Reset Control

NAME	TERMINAL	UNIT	DESCRIPTION
RetryDisable	VIDPIX18	PCI	1 = do not attempt retries
DeltaEnable	VIDPIX17	PCI	1 = enable delta aperture
ShortReset	VIDPIX16	PCI	1 = use short reset
AuxEnable	VIDPIX14	PCI	Set to zero
AuxIOEnable	VIDPIX13	PCI	Set to zero
MClkPeriod3	VIDPIX11	PCI	Bit 3 of MCLK period (ns – 10)
MClkPeriod2	VIDPIX10	PCI	Bit 2 of MCLK period (ns – 10)
MClkPeriod1	VIDPIX9	PCI	Bit 1 of MCLK period (ns – 10)
MClkPeriod0	VIDPIX8	PCI	Bit 0 of MCLK period (ns – 10)
PCIMaxLat1	VIDPIX7	PCI	Bit 7 of PCI max latency register
PCIMaxLat0	VIDPIX6	PCI	Bit 6 of PCI max latency register
PCIMinLatency1	VIDPIX5	PCI	Bit 7 of PCI min grant register
PCIMinLatency0	VIDPIX4	PCI	Bit 6 of PCI min grant register
BaseClassZero	VIDPIX3	PCI	1 = base class is zero
VgaEnable	VIDPIX1	PCI	1 = VGA present
VgaFixed	VIDPIX0	PCI	1 = enable VGA fixed address
SDRAM	MDAT46	MEM	1 = support SDRAM
Burst1Cycle	MDAT45	MEM	1 = single burst
BankDelay2	MDAT44	MEM	Bit 2 of bank delay count

Table 2–73. Reset Control (Continued)

NAME	TERMINAL	UNIT	DESCRIPTION
BankDelay1	MDAT43	MEM	Bit 1 of bank delay count
BankDelay0	MDAT42	MEM	Bit 0 of bank delay count
DeadCycle	MDAT41	MEM	1 = dead cycle between rd and wr
TimeRASMin2	MDAT40	MEM	Bit 2 of tRAS minimum parameter
TimeRASMin1	MDAT39	MEM	Bit 1 of tRAS minimum parameter
TimeRASMin0	MDAT38	MEM	Bit 0 of tRAS minimum parameter
RefreshCount7	MDAT37	MEM	Bit 7 of refresh count
RefreshCount6	MDAT36	MEM	Bit 6 of refresh count
RefreshCount5	MDAT35	MEM	Bit 5 of refresh count
RefreshCount4	MDAT34	MEM	Bit 4 of refresh count
RefreshCount3	MDAT33	MEM	Bit 3 of refresh count
RefreshCount2	MDAT32	MEM	Bit 2 of refresh count
RefreshCount1	MDAT31	MEM	Bit 1 of refresh count
RefreshCount0	MDAT30	MEM	Bit 0 of refresh count
NumberBanks1	MDAT29	MEM	Bit 1 of number of banks
NumberBanks0	MDAT28	MEM	Bit 0 of number of banks
BootAddress9	MDAT27	MEM	Bit 9 of SGRAM boot address
BootAddress8	MDAT26	MEM	Bit 8 of SGRAM boot address
BootAddress7	MDAT25	MEM	Bit 7 of SGRAM boot address
BootAddress6	MDAT24	MEM	Bit 6 of SGRAM boot address
BootAddress5	MDAT23	MEM	Bit 5 of SGRAM boot address
BootAddress4	MDAT22	MEM	Bit 4 of SGRAM boot address
BootAddress3	MDAT21	MEM	Bit 3 of SGRAM boot address
BootAddress2	MDAT20	MEM	Bit 2 of SGRAM boot address
BootAddress1	MDAT19	MEM	Bit 1 of SGRAM boot address
BootAddress0	MDAT18	MEM	Bit 0 of SGRAM boot address
CAS3Latency	MDAT17	MEM	1 = CAS latency 3 clocks
TimeRP2	MDAT16	MEM	Bit 2 of tRP parameter
TimeRP1	MDAT15	MEM	Bit 1 of tRP parameter
TimeRP0	MDAT14	MEM	Bit 0 of tRP parameter
TimeRC3	MDAT13	MEM	Bit 3 of tRC parameter
TimeRC2	MDAT12	MEM	Bit 2 of tRC parameter
TimeRC1	MDAT11	MEM	Bit 1 of tRC parameter
TimeRC0	MDAT10	MEM	Bit 0 of tRC parameter
TimeRCD2	MDAT9	MEM	Bit 2 of tRCD parameter
TimeRCD1	MDAT8	MEM	Bit 1 of tRCD parameter
TimeRCD0	MDAT7	MEM	Bit 0 of tRCD parameter
BoardConfig1	MDAT6	MEM	Bit 1 of BoardConfig value
BoardConfig0	MDAT5	MEM	Bit 0 of BoardConfig value

Table 2–74. Reset Control (Continued)

NAME	TERMINAL	UNIT	DESCRIPTION
RowCharge	MDAT4	MEM	1 = enable row charge
TimeRPW3	MDAT3	MEM	Bit 3 of ROM pulse width
TimeRPW2	MDAT2	MEM	Bit 2 of ROM pulse width
TimeRPW1	MDAT1	MEM	Bit 1 of ROM pulse width
TimeRPW0	MDAT0	MEM	Bit 0 of ROM pulse width

3 Electrical Characteristics

3.1 Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 3.8 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{DD} + 0.3 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
dc supply voltage, V_{CC} . . . . . 5 V
I/O Voltage with respect to GND . . . . . –0.5 V to V_{DD} + 0.3 V
I/O Voltage with respect to GND (see Note 2) . . . . . –0.5 V to V_{CC}+ 0.5 V
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C
Junction temperature range, T_J . . . . . 125°C
Case temperature range for 10 seconds, T_C . . . . . 260°C
Lead temperature range 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to GND.
2. Applies to the following signals: PCIAD(0–31), $\overline{\text{PCICBE}}$(0–3), PCIPAR, $\overline{\text{PCIFRAME}}$, $\overline{\text{PCIFRAME}}$, $\overline{\text{PCIIRDY}}$, $\overline{\text{PCISTOP}}$, $\overline{\text{PCILOCK}}$, $\overline{\text{PCIIDSEL}}$, $\overline{\text{PCIDEVSEL}}$, $\overline{\text{PCIREQ}}$, $\overline{\text{PCIGNT}}$, $\overline{\text{PCIINTA}}$, PCICIK, PCIFIFOINDIS, PCIFIFOOUTDIS, $\overline{\text{PCIRST}}$, DDC, $\overline{\text{AUXWAIT}}$, VCLK, MCLK, and RDACDAT (0–7).

3.2 Recommended Operating Conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	3.3	3.6	V
Supply voltage, V_{CC}	4.75	5.0	5.25	V
High-level input voltage, V_{IH}	2.0		V_{DD}+0.8	V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature range, T_A	0		70	°C

3.3 Electrical Characteristics

PARAMETER		TEST CONDITIONS	TVP4010–60			TVP4010–80			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
L	Inductance				18.4			18.4	nH
I_{CC}	Supply current (running Direct3D game)	V_{CC} = 3.3 V		0.5			0.7		A

3.3.1 PCI

PARAMETER		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage			0.8	V
V_{IH}	High-level input voltage	2.0			V
V_{OL}	Low-level output voltage			0.5	V
V_{OH}	High-level output voltage	2.4			V
I_{IL}	Low-level input current			–20	µA
I_{IH}	High-level input current			20	µA
C_I	Input capacitance			10	pF
$C_{I(CLK)}$	Input capacitance, PCI clock			10	pF
$C_{I(DSEL)}$	Input capacitance, PCI IDSEL			8	pF

3.3.2 Non-PCI

PARAMETER		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage			0.8	V
V_{IH}	High-level input voltage	2.0			V
V_{OL}	Low-level output voltage			0.5	V
V_{OH}	High-level output voltage	2.4			V
I_{IL}	Low-level input current			1	µA
I_{IH}	High-level input current			1	µA
$I_{IH(PD)}$	High-level input current, pulldown			250	µA
$I_{IL(PU)}$	Low-level input current, pullup			250	µA
C_I	Input capacitance			10	pF

3.4 Operating Characteristics

			MIN	TYP	MAX	UNIT
C_L	Capacitive load	MADD(0–9)	80	80	80	pF
		PCIAD(0–31), $\overline{\text{PCICBE}}$(0–3), PCIPAR, $\overline{\text{PCIFRAME}}$, $\overline{\text{PCIIRDY}}$, $\overline{\text{PCITRDY}}$, $\overline{\text{PCISTOP}}$, PCIIDSEl, $\overline{\text{PCIDEVSEl}}$, $\overline{\text{PCIREQ}}$, $\overline{\text{PCIGNT}}$, $\overline{\text{PCIINTA}}$, MBANK(0–3), MBYTE(0–7), MCAS(0–1), MDSF(0–1), MEMCKE, $\overline{\text{MEMCKOUT}}$(0–1), $\overline{\text{MRAS}}$(0–1), MWE(0–1), $\overline{\text{RAMDACR}}$, $\overline{\text{RAMDACW}}$, RDACADD(0–3), RDACDAT(0–7)	50	50	50	pF
		MDAT(60–63)	40	40	40	pF
		$\overline{\text{AUXREAD}}$, $\overline{\text{AUXWRITE}}$, RESETOUT, $\overline{\text{ROM}}$, $\overline{\text{ROMWE}}$, VIDBLANK, VIDCTL(0–1), VIDPIX(0–31)	30	30	30	pF
		VIDHSYNC, VIDVSYNC	20	20	20	pF

3.5 Timing Requirements

PARAMETER		TVP4010–60			TVP4010–80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{c1}	Cycle time, PCICLK	30			30			ns
t_{w1}	Pulse duration, PCICLK high	12			12			ns
t_{w2}	Pulse duration, PCICLK low	12			12			ns
t_{c2}	Cycle time, MCLK	16.7			12.5			ns
t_{w3}	Pulse duration, MCLK high	6.5			5			ns
t_{w3}	Pulse duration, MCLK low	6.5			5			ns
t_{c3}	Cycle time, VCLK	12.5			12.5			ns
t_{w4}	Pulse duration, VCLK high	5			5			ns
t_{w5}	Pulse duration, VCLK low	5			5			ns

3.5.1 PCI Clock Referenced Input Timing

PARAMETERS			MIN	TYP	MAX	UNIT
t_{su1}	Setup time	PCIAD(0–31), $\overline{\text{PCICBE}}$(0–3), PCIPAR, $\overline{\text{PCIFRAME}}$, PCIIRDY, PCITRDY, PCISTOP, PCIIDSEL, PCIDEVSEl	7			ns
		$\overline{\text{PCIGNT}}$	10			ns
		$\overline{\text{PCIRST}}$ (see Note 1)	7			ns
		RDACDATA(0–7)	13			ns
t_{h1}	Hold time	PCIAD(0–31), $\overline{\text{PCICBE}}$(0–3), PCIPAR, $\overline{\text{PCIFRAME}}$, PCIIRDY, PCITRDY, PCISTOP, PCIIDSEL, $\overline{\text{PCIDEVSEl}}$	0			ns
		$\overline{\text{PCIGNT}}$	0			ns
		$\overline{\text{PCIRST}}$ (see Note 1)	0			ns
		RDACDATA(0–7)	2			ns

NOTE 1: $\overline{\text{PCLRST}}$ is resynchronized internally. The timings given, when met, ensure that the reset is detected in the current cycle.

3.5.2 PCI Clock Referenced Output Timing

PARAMETERS			MIN	TYP	MAX	UNIT
t_{su2}	Setup time	PCIAD(0–31), $\overline{\text{PCICBE}}$(0–3), PCIPAR, $\overline{\text{PCIFRAME}}$, PCIIRDY, PCITRDY, PCISTOP, PCIIDESL, PCIDEVSEl	2		11	ns
		$\overline{\text{PCIREQ}}$	2		12	ns
		$\overline{\text{PCIINTA}}$ (see Note 2)	2		12	ns

NOTE 2: Timings given are for falling edges of the open drain signal. Rise times are dependent on the value of the external pull-up resistors.

3.5.3 RAMDAC Timing, 33 MHz PCI Clock

PARAMETER		MIN	TYP	MAX	UNITS
t_{w6}	Pulse duration, $\overline{\text{RAMDACW}}$ low		120		ns
t_{su3}	Setup time, address		30		ns
t_{h2}	Hold time, address		30		ns
t_{su4}	Setup time, data		30		ns
t_{h3}	Hold time, data		30		ns
t_{a1}	Access time, data from $\overline{\text{RAMDACR}}$		100		ns
t_{d1}	Delay time, $\overline{\text{RAMDACR}}$ high to data bus three-state		30		ns

3.5.4 AUX Timings, 33 MHz PCI Clock

PARAMETER		MIN	TYP	MAX	UNITS
t_{w7}	Pulse duration, $\overline{\text{AUXREAD}}$ low		150		ns
t_{d2}	Delay time, strobe low to $\overline{\text{AUXWAIT}}$ asserted		30		ns
t_{d3}	Delay time, $\overline{\text{AUXWAIT}}$ high to $\overline{\text{AUXWRITE}}$ high		30		ns
t_{d4}	Delay time, $\overline{\text{AUXWAIT}}$ high to read data valid		0		ns
t_{a2}	Access time, data from $\overline{\text{AUXREAD}}$		130		ns
t_{d2}	Delay time, $\overline{\text{AUXREAD}}$ high to data bus three-state		30		ns

3.5.5 MEMCKOUT Referenced Input Timing

PARAMETERS		TVP4010–60			TVP4010–80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{su5}	Setup time, MDAT(0–63) (see Note 3)	1			1			ns
t_{h5}	Hold time, MDAT(0–63) (see Note 3)	3			2			ns

NOTE 3: All timings below are with respect to MEMCKOUT, which is a delayed version of MCLK.

3.5.6 MEMCKOUT Referenced Output Timing

PARAMETER		TVP4010–60			TVP4010–80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{su6}	Setup time, all memory control, data and address lines (see Note 3)			13.5			9	ns

4 Parameter Measurement Information

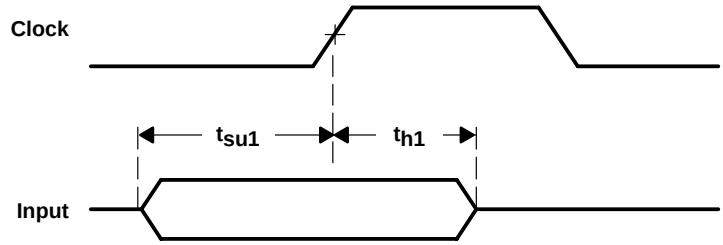


Figure 4–1. Input Timing Parameters

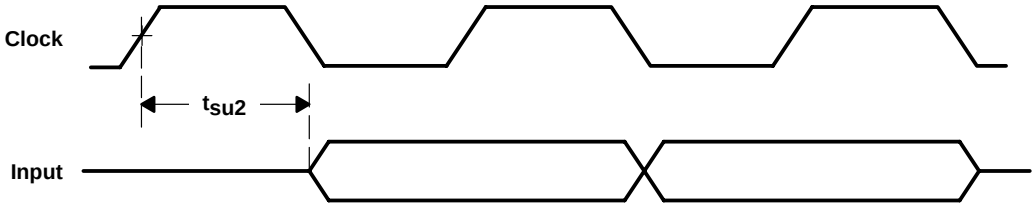


Figure 4–2. Output Timing Parameters

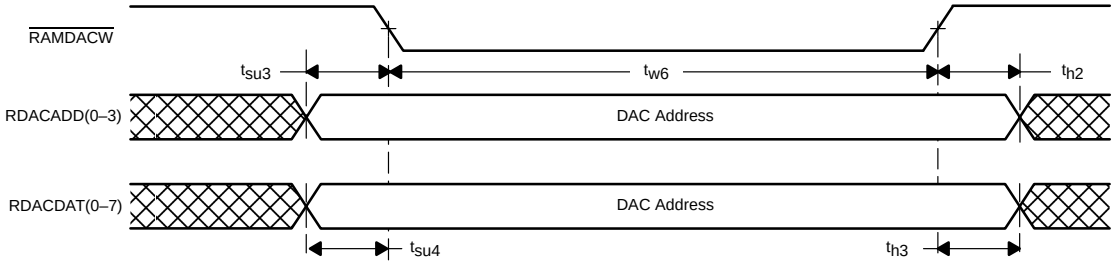


Figure 4–3. DAC Write Timing

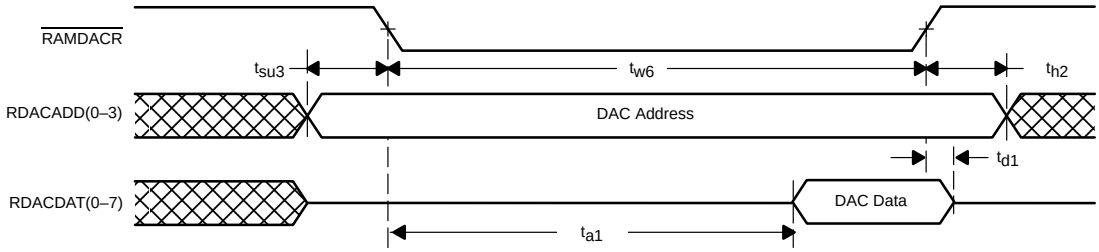


Figure 4–4. DAC Read Timing

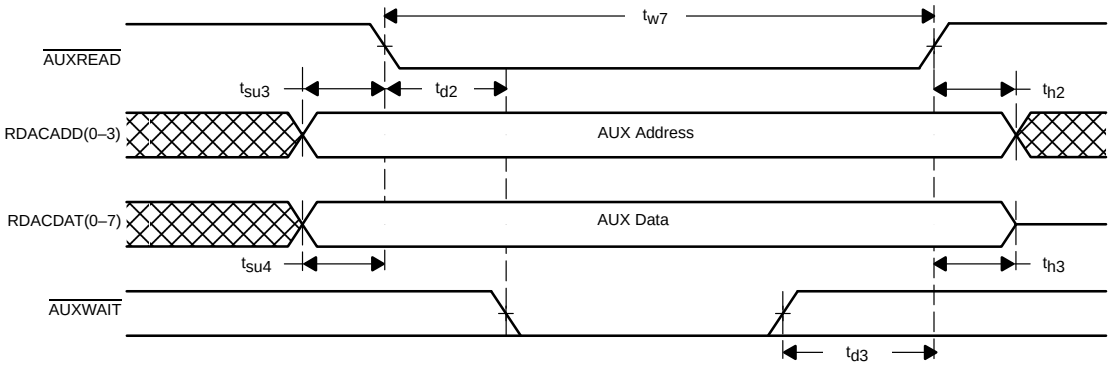


Figure 4–5. AUX Write Timing

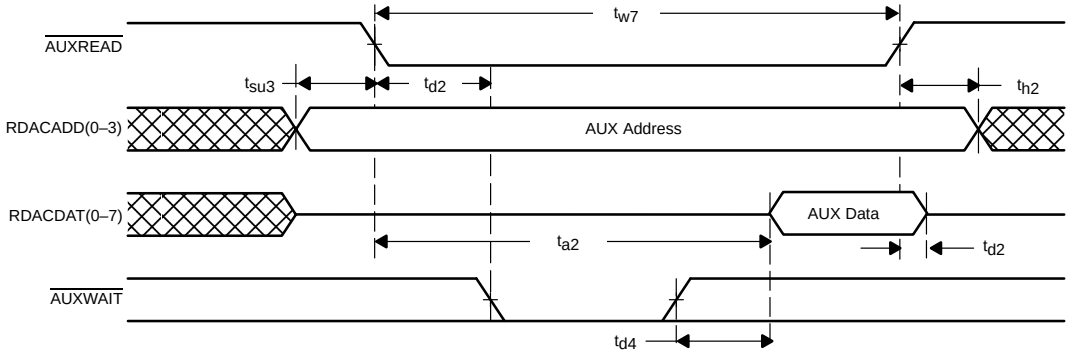


Figure 4–6. AUX Read Timing

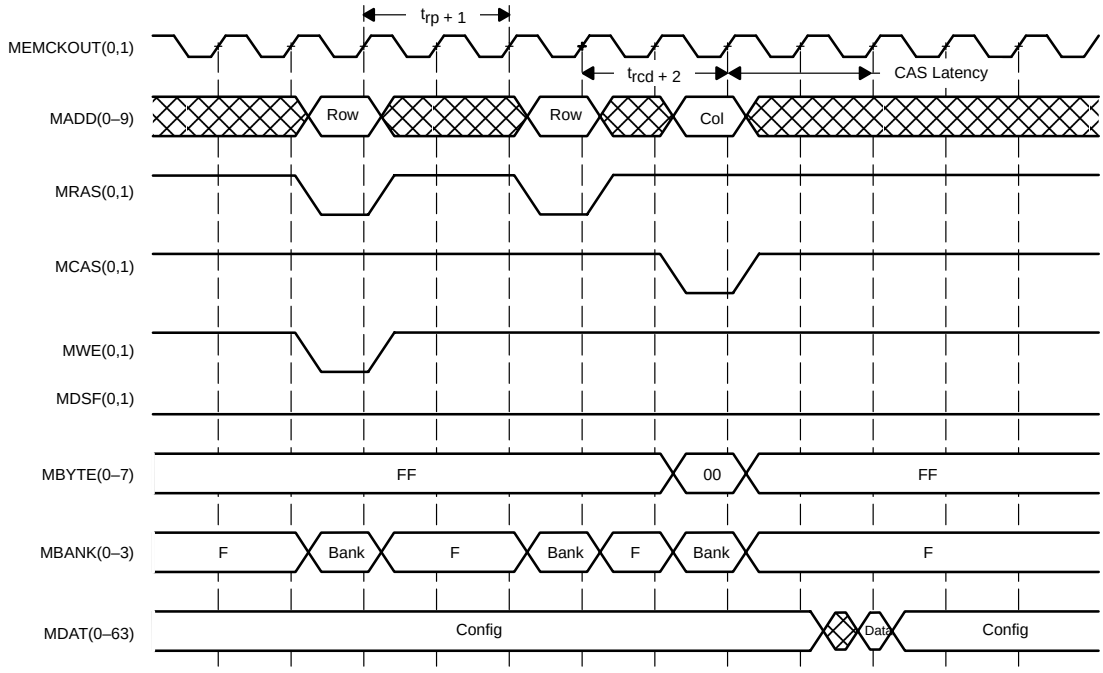


Figure 4–7. Single Read with Precharge Timing

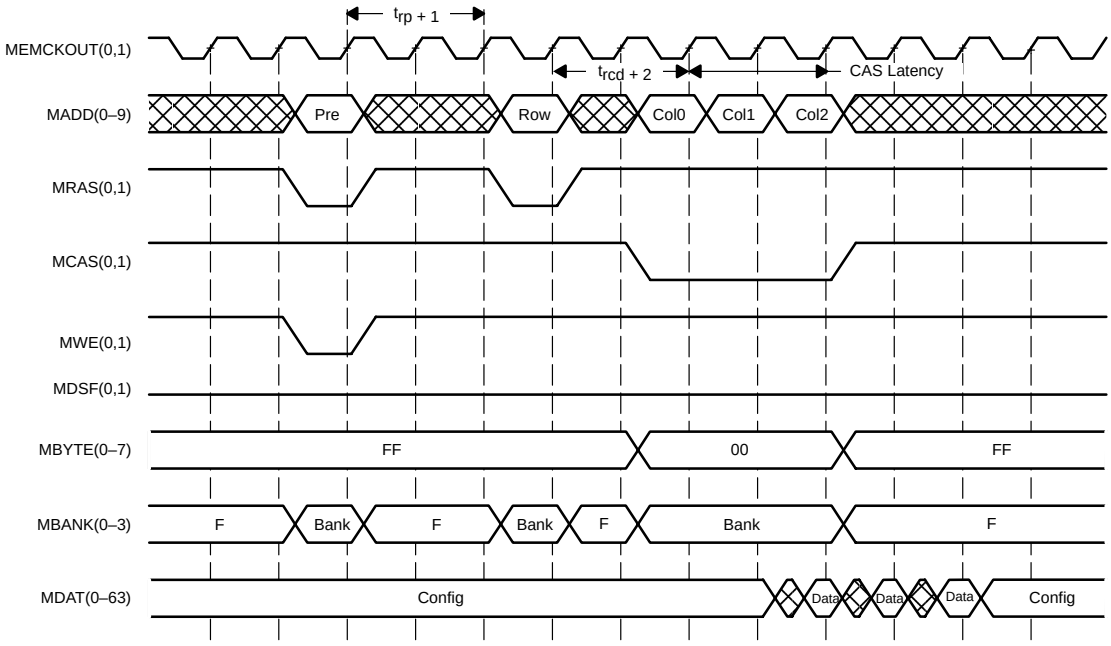


Figure 4–8. Multiple Reads to Same Bank Timing

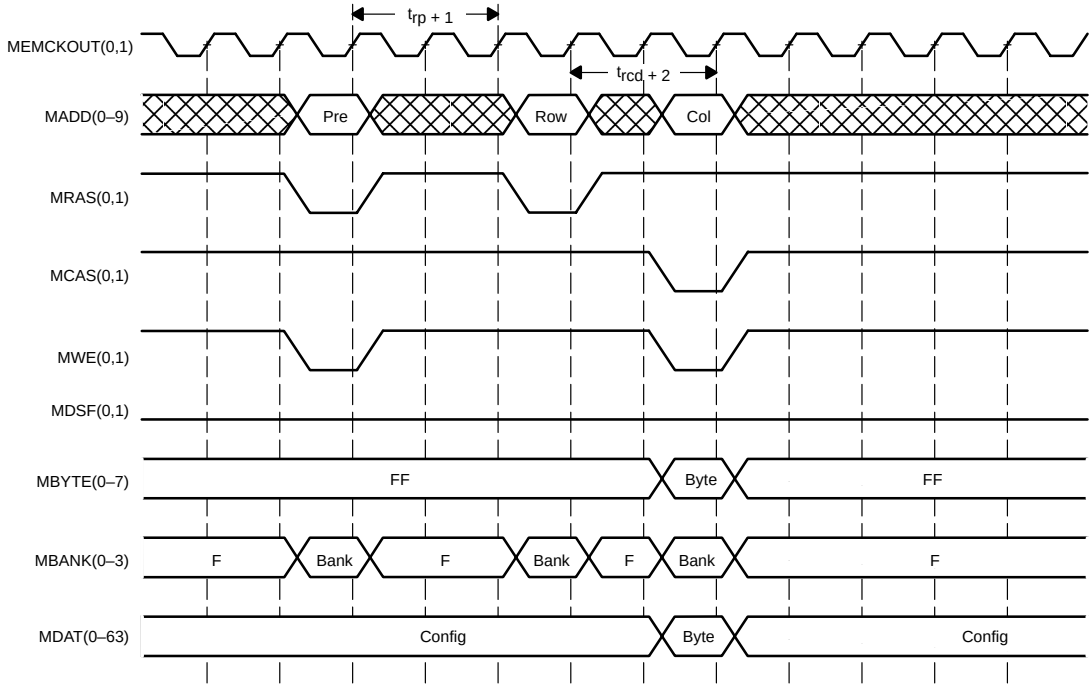


Figure 4–9. Single Write with Precharge Timing

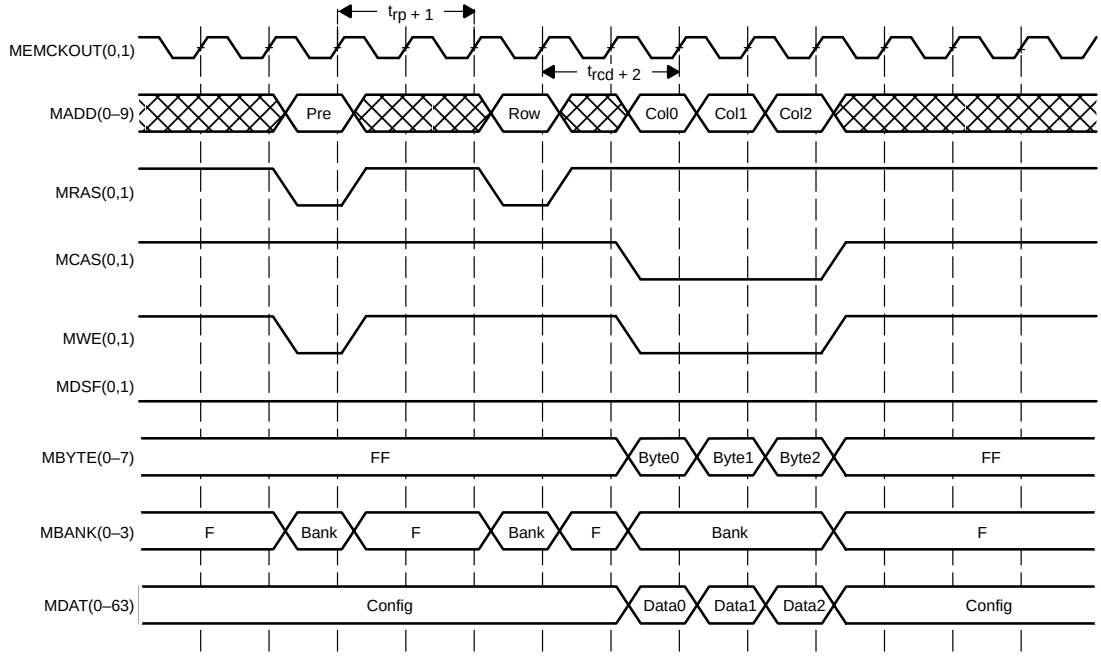


Figure 4–10. Multiple Writes to Same Bank Timing

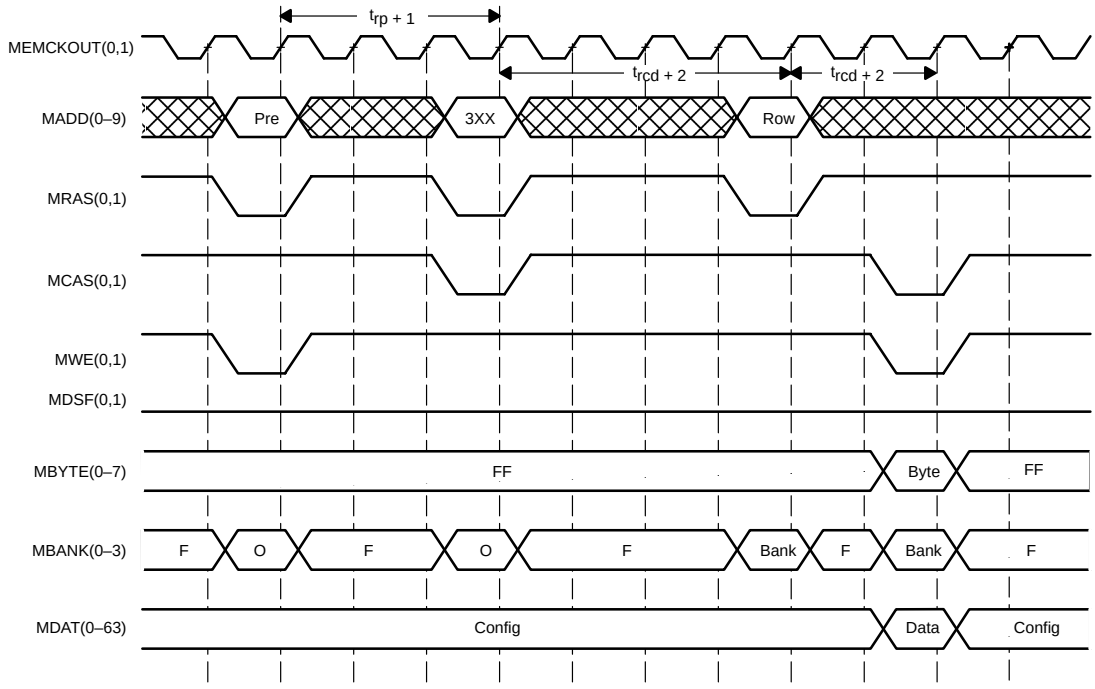


Figure 4–11. Refresh Followed by Access Timing

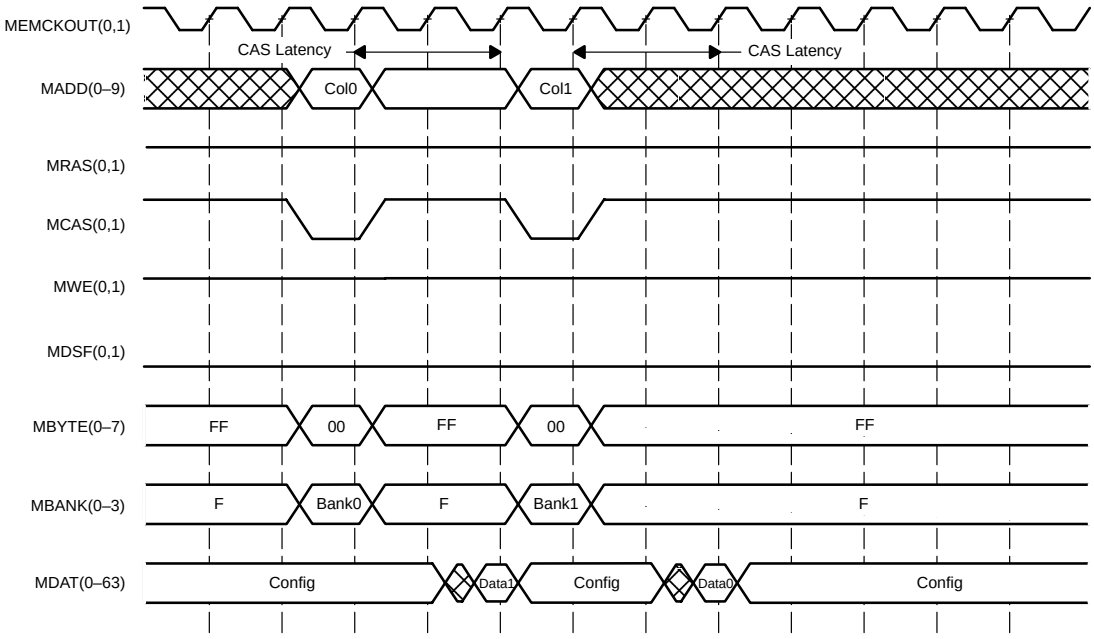


Figure 4–12. Multiple Reads From Different Banks Timing

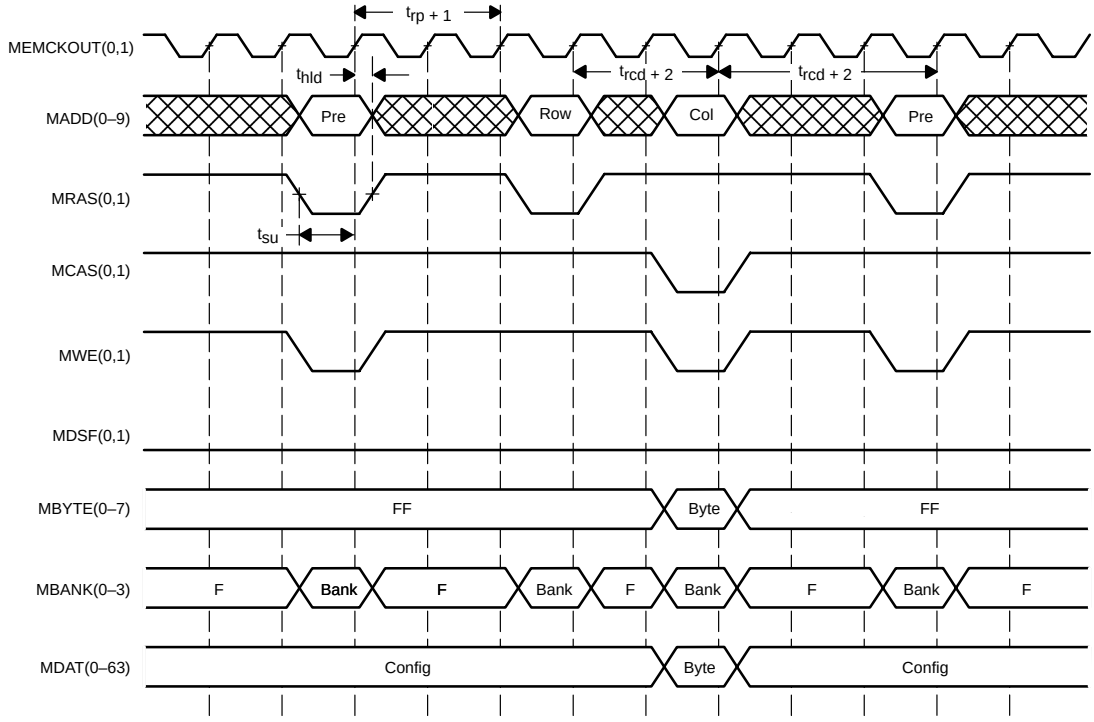


Figure 4–13. RAS Minimum Access Timing

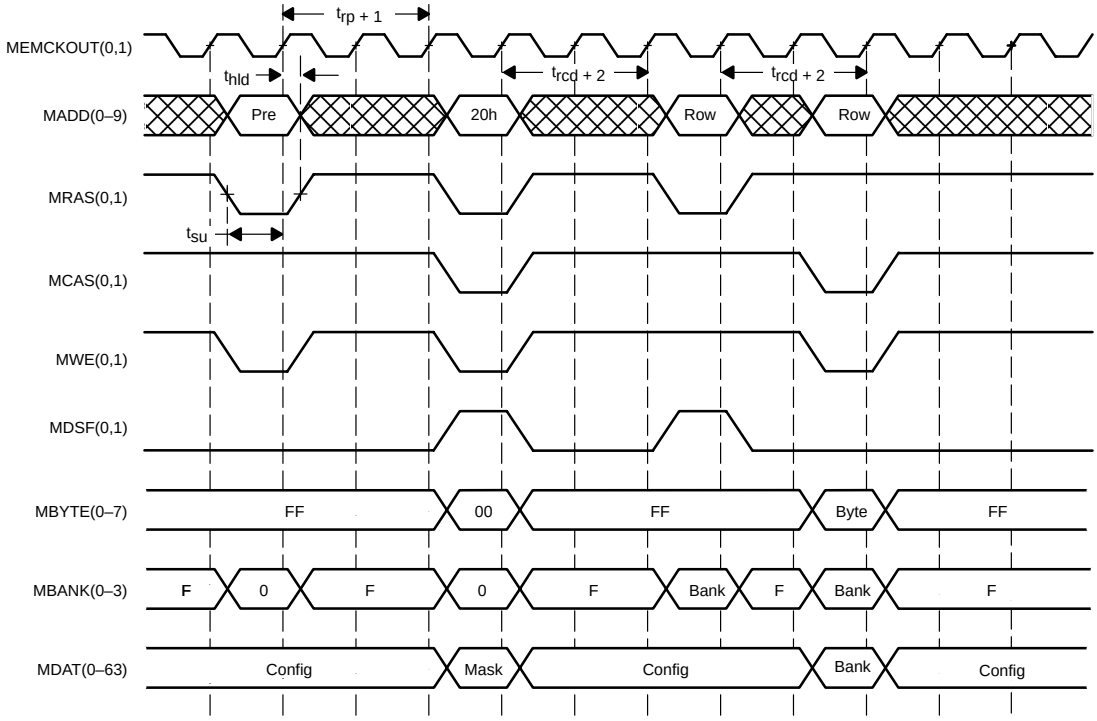


Figure 4–14. Mask Load Followed by Masked Write Timing

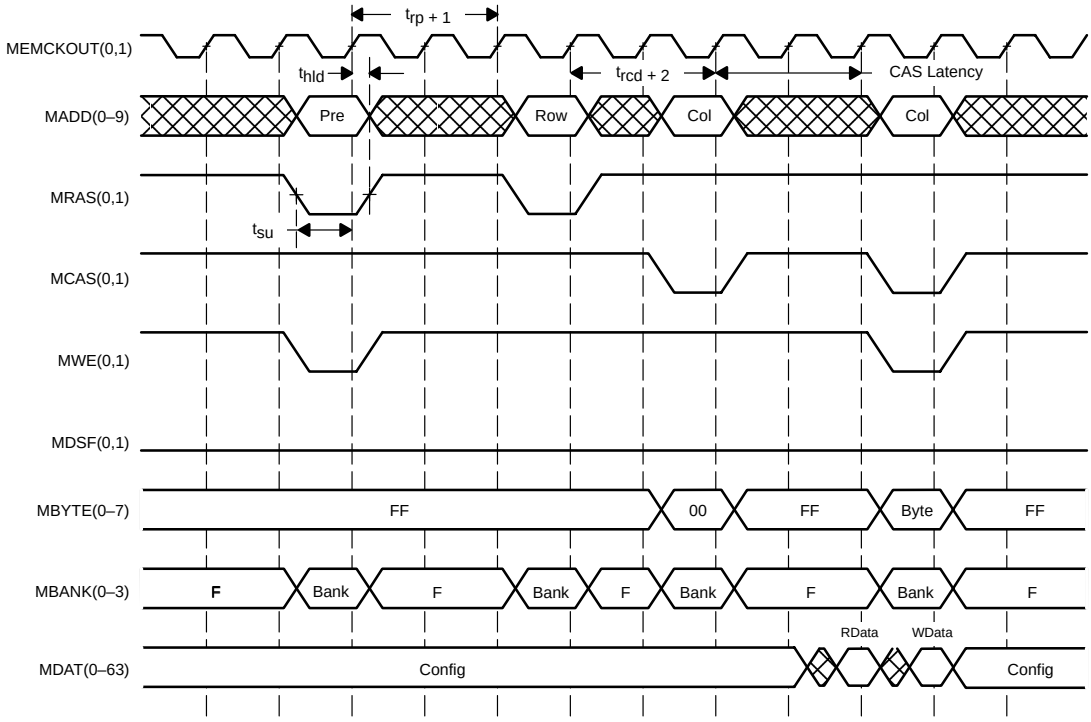


Figure 4–15. Read Followed by Write - No Dead Cycle Timing

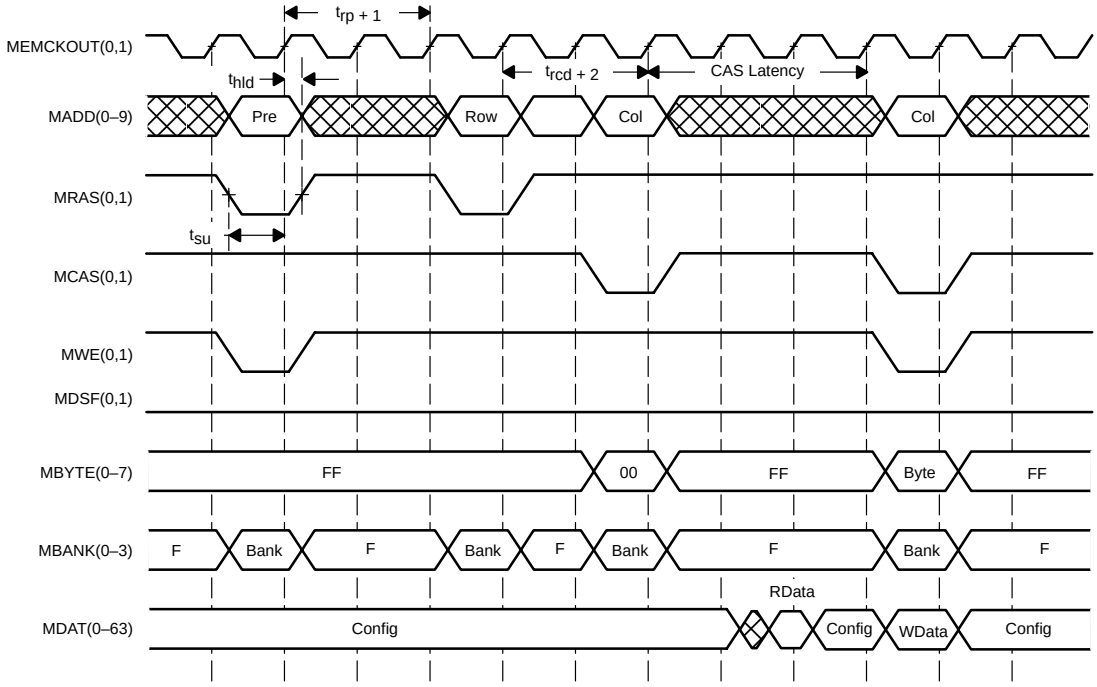


Figure 4–16. Read Followed by Write - With Dead Cycle Timing

5 Application Information

5.1 Video Unit

Figure 5–1 shows the typical organization of a RAMDAC with internal clock generator. The RAMDAC generates a system clock which used by the TVP4010 as the MCLK input. The RAMDAC also generates a video clock which the TVP4010 uses as the VCLK input; this clock is also fed back to the RAMDAC as the load clock. The video clock frequency can be controlled by the TVP4010 with the VCLKCTL terminals.

The pixel data from the TVP4010 is wired directly to the RAMDAC, with the lower 8 bits of the pixel bus spurred off to the RAMDAC VGA pixel inputs. The sync and blank signals are taken directly to the RAMDAC.

The RAMDAC is programmed through the processor interface which has a separate address and data bus from the TVP4010 .

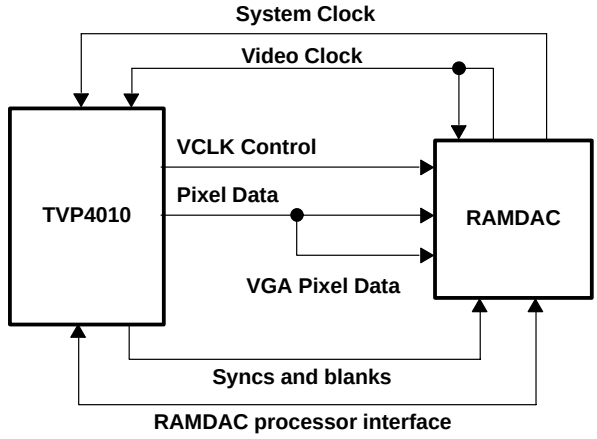


Figure 5–1. Typical RAMDAC Organization

Appendix A
Thermal Characteristics

The maximum junction temperature must be kept below $T_{j(max)}$ and this can only be ensured by proper analysis of the operating environment and the thermal path between the die and the surrounding air.

Device Characteristics

The following characteristics of the device are fixed and are independent of the operating environment or the characteristics of any heatsink:

$T_{J(max)}$	=	125°C
$P_{D(max)}$	=	3.0 Watts @ V_{DD}(max), f_{MCLK} = 50 MHz
Θ_{jc}	=	5.5 °C/Watt

Thermal Model

The formula used to calculate the junction temperature (T_J) is

$$T_J = T_A + P_D(\Theta_{jc} + \Theta_{cs} + \Theta_{jcsa})$$
$$= T_A + P_{D\Theta ja}$$

Where:

T_J	=	Junction temperature (°C)
T_A	=	Ambient temperature (°C)
P_D	=	Power dissipation (Watts)
Θ_{jc}	=	Junction to case thermal resistance (°C/Watt)
Θ_{cs}	=	Case to heatsink thermal resistance (°C/Watt)
Θ_{sa}	=	Heatsink to air thermal resistance (°C/Watt)
Θ_{ja}	=	Total junction to air thermal resistance (°C/Watt)

The Θ_{ja} form of the equation is more appropriate when a heatsink is not attached to the device (see Section *Operation Without Heatsink*).

Operation Without Heatsink

The 256-terminal BGA package without an attached heatsink has the following Θ_{ja} characteristic as a function of airflow:

Table F–1. Airflow Characteristics

AIRFLOW LFPM (LINEAR FEET PER MINUTE)	Θ_{JA} °C/W
0 (Convection Cooling)	26.5
100 (0.5 m/sec)	23
400 (2.0 m/sec)	19

Example:

T_A = 40°C
Airflow = 0 lfpm
T_J = 40+ 3.0 x 26.5
= 119.5°C

Operation With Heatsink

With a heatsink attached to the device, the junction temperature depends on Θ_{cs} and Θ_{sa}. Θ_{cs} is the thermal resistance of the join between the heatsink and the case. Θ_{sa} is the thermal resistance of the heatsink and is a function of system airflow.

Example:

T_A = 40°C
Θ_{cs} = 0.6°C/Watt (EG 7655 epoxy – see Section *Heatsink Attachment*)
Θ_{sa} = (125 – 40)/3.0 – 5.5 – 0.6
= 22.2°C/Watt

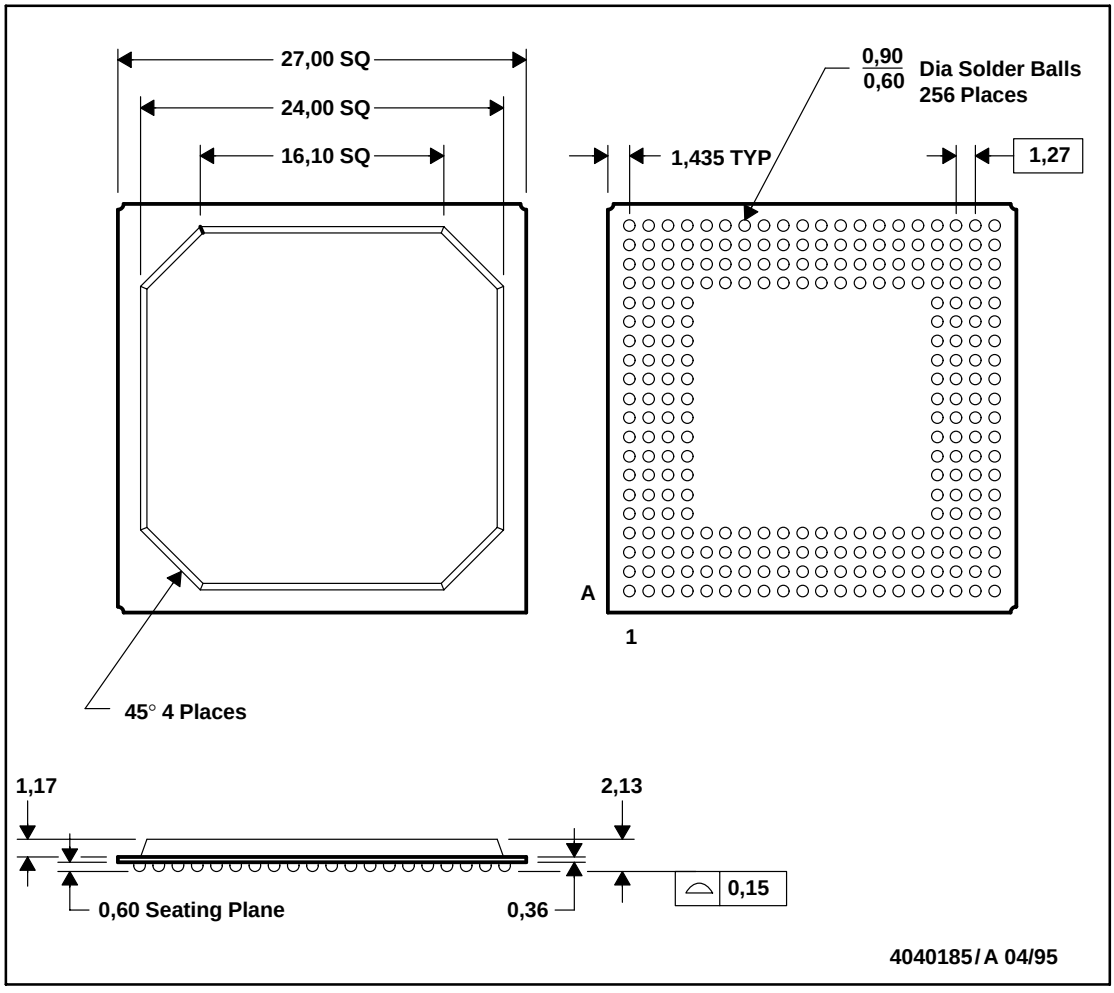
Heatsink Attachment

The heatsink should be attached with a suitable thermally conductive epoxy such as EG 7655 from A.I. Technology Inc. The thickness of the epoxy layer should be between 0.05 mm and 0.15 mm with 100% coverage of the case area, and a maximum voiding in the bond area of 3%.

Typical achievable Θ_{cs} using this method is 0.6°C/Watt.

Appendix B
Mechanical Data

GFN (S-PBGA-N256) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.