CS4610/11

Preliminary Product Bulletin

CrystalClear™ SoundFusion™ PCI Audio Accelerator

FEATURES

- **High Performance PCI Audio Accelerator**
  - — Powerful RAM-based SLIMD™ DSP core provides high task concurrency and maximum flexibility
  - — Efficient bus mastering PCI interface minimizes host loading
  - — DMA engine with hardware scatter-gather manages up to 96 simultaneous audio/data streams
- **Flexible Digital Audio Interface Design**
  - — Direct Connection to CS423XB Codec
  - — Simple expansion to 6 audio output channels
  - — Direct Connection to CS4297 AC'97 Codec
- **Complete Solution including DSP Software and Windows® 95 drivers**
  - — Acceleration of DirectSound®, DirectSound3D®, DirectInput®, and ActiveMovie™ APIs
  - — High Quality HRTF-Based 3D Positional Sound
  - — General MIDI Wavetable Synthesis with Reverb and Chorus
  - — Dolby® AC-3® (5.1 channel), Dolby Pro Logic®, and MPEG-2 Audio Decoding (CS4610 only)

DESCRIPTION

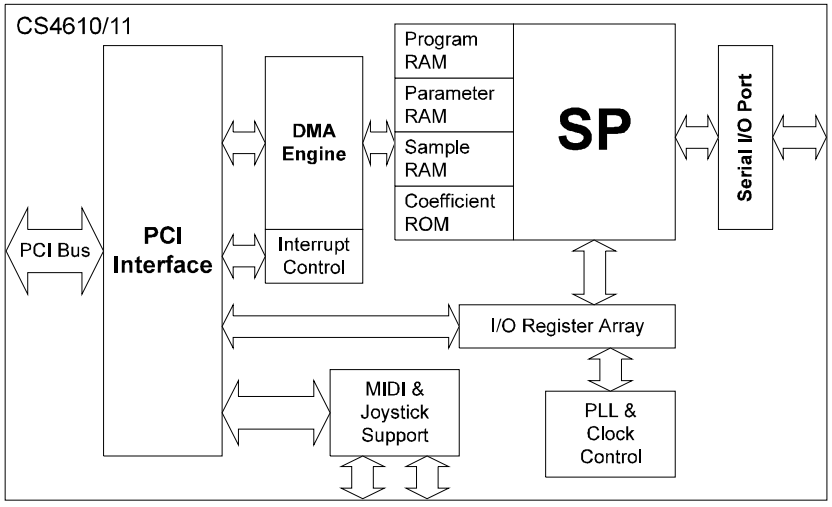
The CS4610/11 is a high performance audio accelerator for the PCI bus. This device, combined with application and driver software from Crystal, provides a complete system solution for hardware acceleration of Windows 95 DirectSound, DirectSound3D, DirectInput, ActiveMovie, and Wavetable Synthesis.

The CS4610/11 is based on the Cirrus Logic, CrystalClear™ Stream Processor (SP) DSP core. The SP core is optimized for digital audio processing, and is powerful enough to handle complex signal processing tasks such as Dolby AC-3 decoding (CS4610 only) with ease. The SP core is supported by a bus mastering PCI interface and a built-in dedicated DMA engine with hardware scatter-gather support. These support functions ensure extremely efficient transfer of audio data streams to and from host-based memory buffers, providing a system solution with maximum performance and minimal host CPU loading.

The all-digital CS4610/11 supports a variety of audio I/O configurations, including direct connection to the CrystalClear™ CS423XB Codec via a proprietary bi-directional serial data link, or direct connection to an AC'97 Codec such as the CrystalClear™ CS4297.

ORDERING INFORMATION

CS4610-CM 100-pin PQFP
CS4611-CM 100-pin PQFP



CIRRUS LOGIC PRELIMINARY PRODUCT BULLETIN

ELECTRICAL SPECIFICATIONS

The electrical information provided in the following tables is currently being validated. Cirrus Logic, Inc. reserves the right to change or update this information without warning. Updates will be provided in future revisions of this document.Timing diagrams for some of these tables are provided in the main section of this document; appropriate page number references are included when appropriate.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	PCIVDD	-	-	4.6	V
	CVDD	-	-	4.6	V
	CRYVDD	-	-	4.6	V
	VDD5REF	-	-	5.5	V
Total Power Dissipation (Note 1)		-	-	1.5	W
Input Current per Pin, DC (Except supply pins)		-	-	10	mA
Output current per pin, DC		-	-	10	mA
Input voltage (Note 2)		-0.3	-	5.75	V
Ambient temperature (power applied) (Note 3)		-45	-	85	°C
Storage temperature		-55	-	150	°C

Notes: 1. Includes all power generated by AC and/or DC output loading.
2. The power supply pins are at recommended maximum values. XTALI & XTALO are at 3.6 V maximum.
3. At Ambient temperatures above 70 °C, total power dissipation must be limited to less than 0.4 Watts.

WARNING: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

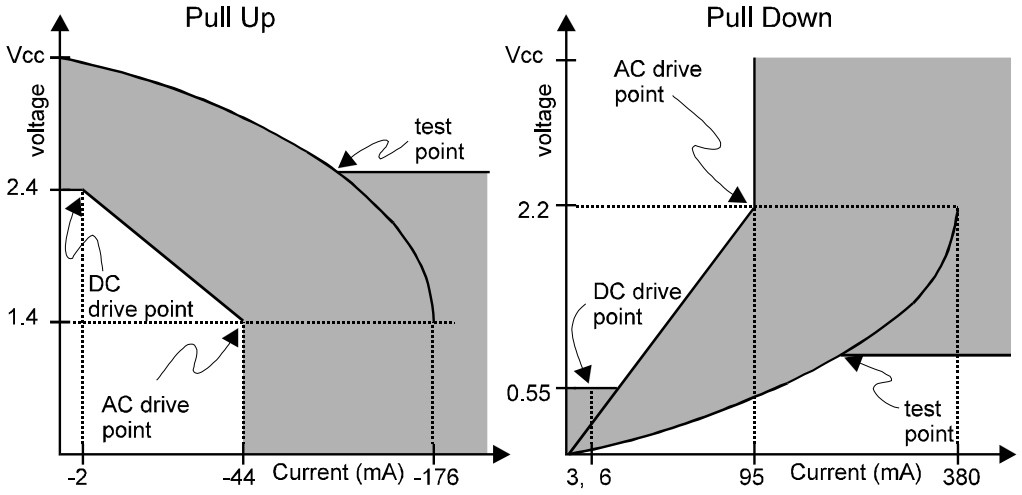
RECOMMENDED OPERATING CONDITIONS (all voltages with respect to GND = 0 V)

		Min	Typ	Max	Min	Typ	Max	
Parameter	Symbol	CS4610			CS4611			Unit
Power Supplies	PCIVDD	3	3.3	3.6	3	3.3	3.6	V
	CVDD	3	3.3	3.6	3	3.3	3.6	V
	CRYVDD	3	3.3	3.6	3	3.3	3.6	V
	VDD5REF	4.75	5	5.25	4.75	5	5.25	V
Internal DSP Frequency		-	-	100	-	-	85	MHz
Operating Ambient Temperature	T_A	0	25	70	0	25	70	°C
PCI Clock Frequency		-	-	33	-	-	33	MHz

AC CHARACTERISTICS (PCI SIGNAL PINS ONLY) (T_A = 70 °C; PCIVDD = CVDD = CRYVDD = 3.3V; VDD5REF = 5V; Logic 0 = 0V, Logic 1 = VDD; output load = 10pF; I/P & O/P timing reference levels = 1.5V; Pulse levels are 0V to 3V; I/P rise & fall time = 2ns; unless otherwise noted; (Note 4))

Parameter			Symbol	Min	Max	Unit
Switching Current High		(Note 5)	I_{OH}			
		0 < Vout < 1.4		-44	-	mA
		1.4 < Vout < 2.4		$-44+\frac{Vout-1.4}{0.024}$	-	mA
		3.1 < Vout < Vcc		-	Note 7	
Switching Current Low		(Note 5)	I_{OL}			
		Vout > 2.2		95	-	mA
		2.2 > Vout > 0.55		Vout/0.023	-	mA
		0.71 > Vout > 0		-	Note 8	
Low Clamp Current		-5 < Vin < -1	I_{CL}	$-25+\frac{Vin+1}{0.015}$	-	mA
Output rise slew rate	0.4V - 2.4V load	(Note 6)	slewr	1	5	V/ns
Output fall slew rate	2.4V - 0.4V load	(Note 6)	slewf	1	5	V/ns

Notes:
4. Specifications guaranteed by characterization and not production testing.
5. Refer to V/I curves in Figure 1. Specification does not apply to CLK and RST# signals. Switching Current High specification does not apply to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.
6. Cumulative edge rate across specified range. Rise slew rates do not apply to open drain outputs.
7. Equation A: I_{OH} = 11.9 * (Vout - 5.25) * (Vout + 2.45) for Vcc > Vout > 3.1V
8. Equation B: I_{OL} = 78.5 * Vout * (4.4 - Vout) for 0V < Vout < 0.71V



Equation A:

$I_{OH} = 11.9*(Vout-5.25)*(Vout+2.45)$ *for Vcc > Vout > 3.1V*

Equation B:

$I_{OL} = 78.5*Vout*(4.4-Vout)$ *for 0V < Vout < 0.71V*

Figure 1. AC Characteristics

DC CHARACTERISTICS (T_A = 70 °C; PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; unless otherwise noted)

Parameter			Symbol	Min	Typ	Max	Unit
PCI Interface Signal Pins							
High level input voltage			V_{IH}	2	-	5.75	V
Low level input voltage			V_{IL}	-0.5	-	0.8	V
High level output voltage	Iout = -2 mA		V_{OH}	2.4	-	-	V
Low level output voltage	Iout = 3 mA, 6 mA	(Note 9)	V_{OL}	-	-	0.55	V
High level leakage current	Vin = 2.7	(Note 10)	I_{IH}	-	-	70	µA
Low level leakage current	Vin = 0.5	(Note 10)	I_{IL}	-	-	-70	µA
Non-PCI Interface Signal Pins (Except XTALI and XTALO)							
High level input voltage			V_{IH}	2	-	5.75	V
Low level input voltage			V_{IL}	-0.5	-	0.8	V
High level output voltage	Iout = -4 mA	(Note 11)	V_{OH}	2.4	-	-	V
Low level output voltage	Iout = 4 mA		V_{OL}	-	-	0.4	V
High level leakage current	Vin = 5.25		I_{IH}	-	-	10	µA
Low level leakage current	Vin = 0		I_{IL}	-	-	-10	µA

Parameter		Min	Typ	Max	Min	Typ	Max	Unit
		CS4610			CS4611			
Power Supply Pins (Outputs Unloaded)								
Power Supply Current (Note 12)	PCIVDD	-	5	-	-	5	-	mA
	CVDD	-	300	-	-	240	-	mA
	CRYVDD	-	10	-	-	8	-	mA
	VDD5REF	-	0.6	-	-	0.6	-	mA
Low Power Mode Supply Current		-	10	-	-	10	-	mA

Notes: 9. Signals without pull-up resistors must have 3mA low output current. Signals requiring pull up must have 6 mA; the latter include FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, INTA#.

10. .Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.

11. For open drain pins high level output voltage dependent on external pull -up used and number of attached gates.

12. Typical values are given as average current with typical SP task execution and data streaming.

TIMING PARAMETERS

PCI INTERFACE PINS

(T_A = 0 to 70 °C; PCIVDD = CVDD = CRYVDD = 3.3V; VDD5REF = 5 V; Logic 0 = 0 V, Logic 1 = VDD; output load = 10 pF; I/P & O/P timing reference levels = 1.5 V; Pulse levels are 0 V to 3 V; I/P rise & fall time = 2 ns; unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
CLK cycle time		t_{cyc}	30	-	ns
CLK high time		t_{high}	11	-	ns
CLK low time		t_{low}	11	-	ns
CLK slew rate	(Note 13)		1	4	V/ns
RST# slew rate	(Note 14)		50	-	mV/ns
CLK to signal valid delay - bused signals	(Note 15)	t_{val}	2	11	ns
CLK to signal valid Delay - point to point	(Note 15)	$t_{val(p+p)}$	2	12	ns
Float to active delay	(Note 16)	t_{on}	2	-	ns
Active to Float delay	(Note 16)	t_{off}	-	28	ns
Input Set up Time to CLK - bused signals		t_{su}	7	-	ns
Input Set up Time to CLK - point to point		$t_{su(p+p)}$	10, 12	-	ns
Input hold time for CLK		t_h	0	-	ns
Reset active Time after power stable	(Note 17)	t_{rst}	1	-	ms
Reset active time after CLK stable	(Note 17)	$t_{rst-clk}$	100	-	us
Reset active to Output Float delay	(Notes 16, 17, 18)	$t_{rst-off}$	-	40	ns

Notes: 13. Slew rate measured across the minimum peak-to-peak portion of the clock waveform.

14. Applies only to the rising edge of the reset signal.

15. Min timings evaluated with 0 pF equivalent load. Max timing evaluated with 50 pF equivalent load.

16. For Active/Float measurements, the Hi-Z or “off” state is when the total current delivered is less than or equal to the leakage current. Specifications are guaranteed by design and not production tested.

17. RST# is asserted and de-asserted asynchronously with respect to CLK.

18. All output drivers are asynchronously floated when RST# is active.

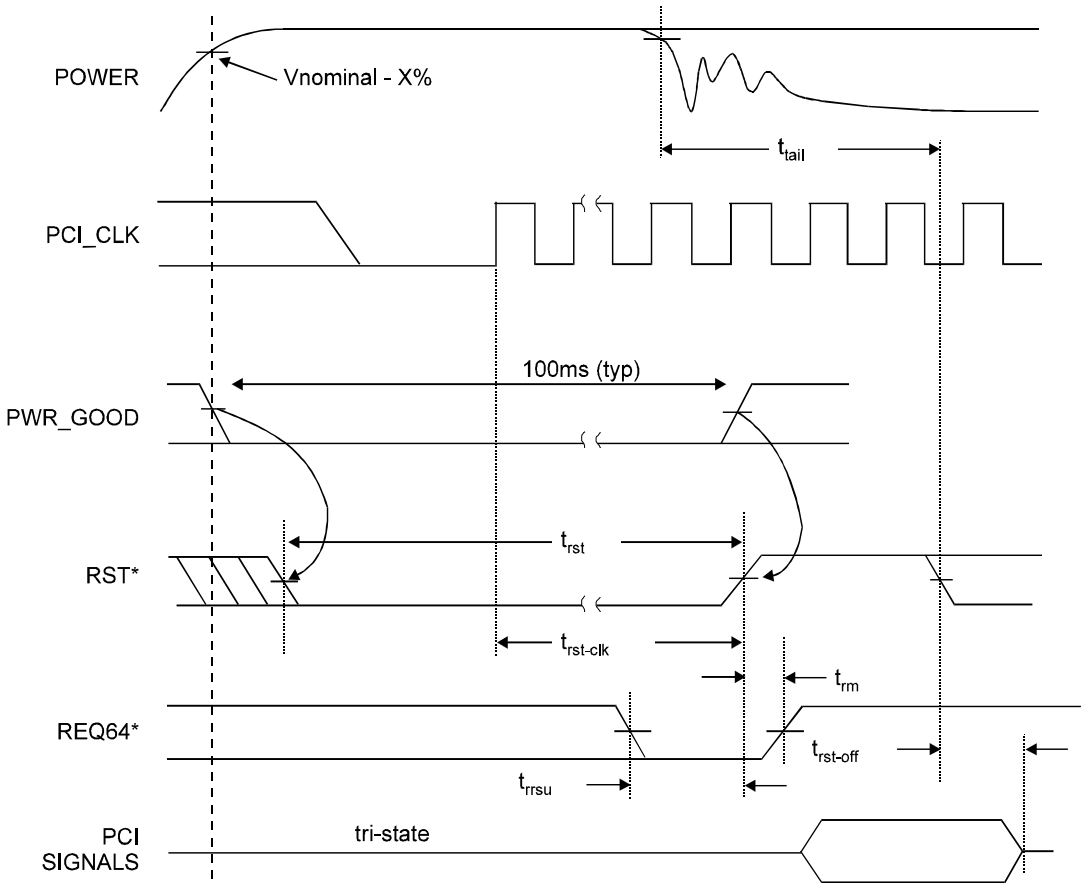


Figure 2. Reset Timing

CS4610/11 + CS423XB CONFIGURATION (T_A = 0 to 70 °C; PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; Logic 0 = 0 V, Logic 1 = VDD; output load = 10 pF; I/P & O/P timing reference levels = 1.5 V; Pulse levels are 0 V to 3 V; I/P rise & fall time = 2 ns; unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time	t_{sclk}	320	354	-	ns
FSYNC cycle time	t_{fsync}	20480	22676	-	ns
SCLK rising to FSYNC transition	t_{pd1}	-20	-	20	ns
SCLK rising to SDOUT valid	t_{pd2}	-	25	45	ns
SDIN valid to SCLK falling	t_{S1}	30	-	-	ns
SDIN hold after SCLK falling	t_{H1}	30	-	-	ns
LRCLK cycle time	t_{lrclk}	20480	22676	-	ns
SCLK falling to LRCLK transition	t_{pd3}	-	25	45	ns
SCLK falling to SDO2/SDO3 valid	t_{pd4}	-	25	45	ns
SDIN2 valid to SCLK rising (CS5330A)	t_{s2}	30	-	-	ns
SDIN2 hold after SCLK rising (CS5330A)	t_{h2}	30	-	-	ns
SDIN2 valid to SCLK falling (CS8412)	t_{s3}	30	-	-	ns
SDIN2 hold after SCLK falling (CS8412)	t_{h3}	30	-	-	ns

AC97 SERIAL INTERFACE TIMING (T_A = 0 to 70 °C; PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; Logic 0 = 0 V, Logic 1 = VDD; output load = 10 pF; I/P & O/P timing reference levels = 1.5 V; Pulse levels are 0 V to 3 V; I/P rise & fall time = 2 ns; unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time	t_{sclk}	78	81.4	-	ns
FSYNC transition to SCLK falling edge	t_{s1}	20	-	-	ns
SCLK rising to SDOUT valid	t_{pd1}	-	25	45	ns
SDIN valid to SCLK falling	t_{s2}	20	-	-	ns
SDIN hold after SCLK falling	t_{h2}	20	-	-	ns
PCI_CLK rising to ARST valid	t_{pd2}	-	25	45	ns

INDEPENDENT TIMING ENVIRONMENT (T_A = 0 to 70 °C; PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; Logic 0 = 0V, Logic 1 = VDD; output load = 10 pF; I/P & O/P timing reference levels = 1.5 V; Pulse levels are 0 V to 3 V; I/P rise & fall time = 2 ns; Crystal frequency = 12.288 MHz; unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
SCLK cycle time	t_{sclk}	312	326	-	ns
FSYNC cycle time (@SCLK falling edge)	t_{fsync}	20000	20833	-	ns
SCLK falling to FSYNC transition	t_{pd1}	-45	2	45	ns
LRCLK cycle time (@ SCLK rising edge)	t_{lrclk}	20000	20833	-	ns
SCLK rising to LRCLK transition	t_{pd2}	-45	2	45	ns
SCLK falling to SDOUT/O2/O3 valid	t_{pd3}	-	2	45	ns
SDIN/2 valid to SCLK rising (CS5330A)	t_{s1}	30	-	-	ns
SDIN/2 hold after SCLK rising (CS5330A)	t_{h1}	30	-	-	ns
SDIN/2 valid to SCLK falling (CS8412)	t_{s2}	30	-	-	ns
SDIN/2 hold after SCLk falling (CS8412)	t_{h2}	30	-	-	ns

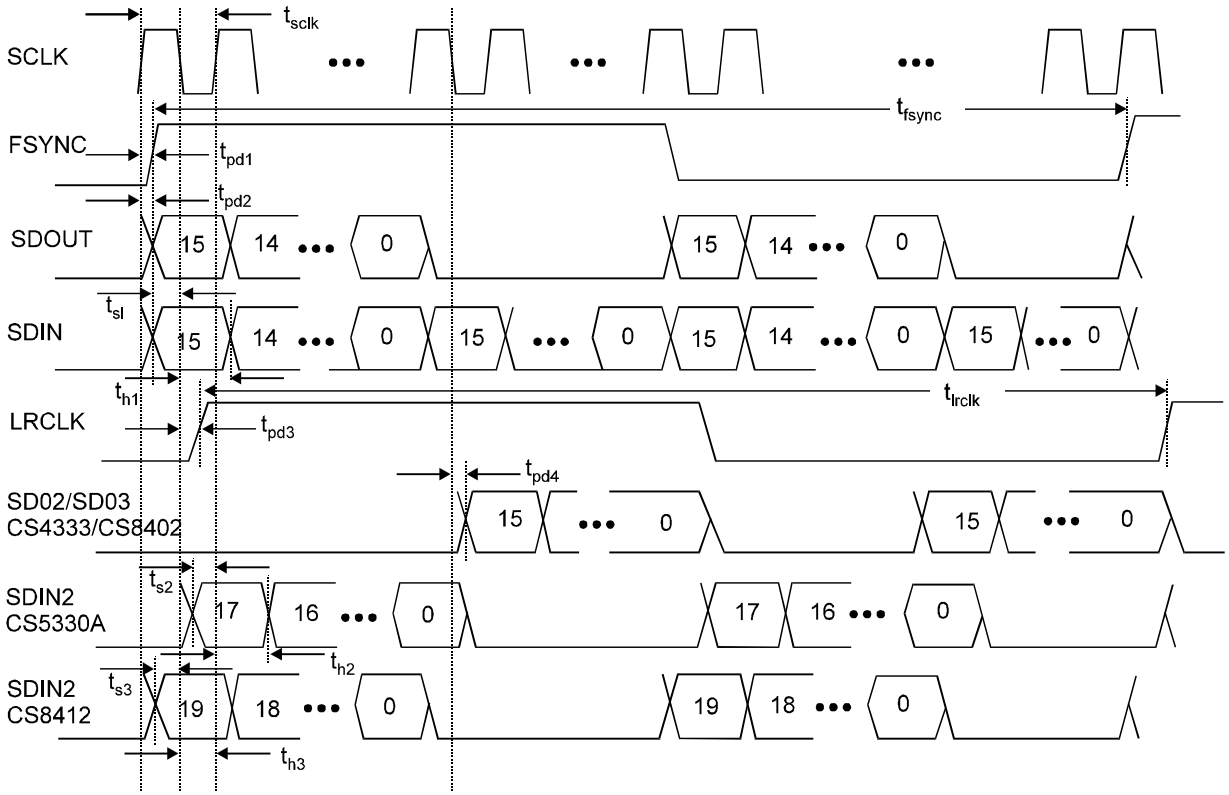


Figure 3. CS4610/11 and CS423XB Link and AC3 Expanded Timing Diagram

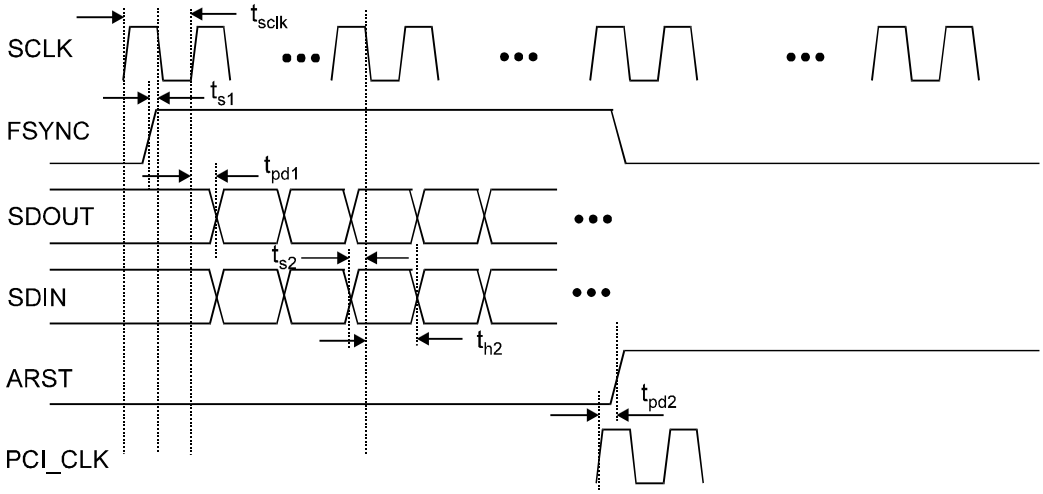


Figure 4. AC97 Configuration Timing Diagram

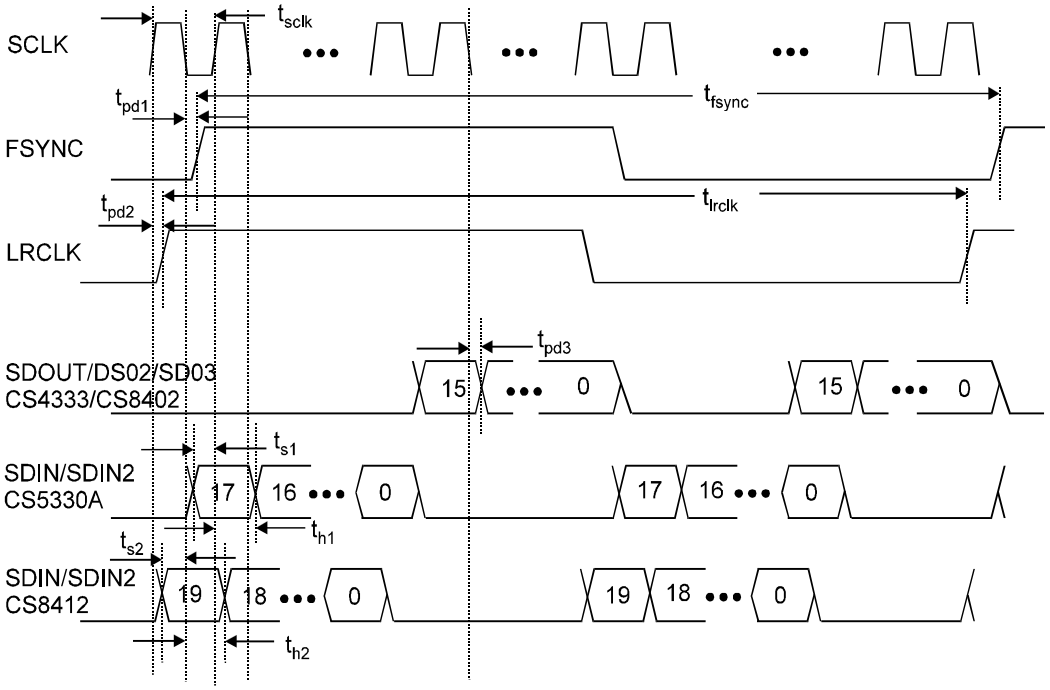


Figure 5. Independent Timing Configuration

EEPROM TIMING CHARACTERISTICS (T_A = 0 to 70 °C, PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; Logic 0 = 0 V, Logic 1 = VDD; output load = 10 pF; I/P & O/P timing reference levels = 1.5 V; Pulse levels are 0 V to 3 V; I/P rise & fall time = 2 ns; PCI clock frequency = 33 MHz; unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Clock frequency (EELCK)	f_{clk}	-	-	41.2	kHz
Clock pulse width low	t_{low}	-	-	12.1	µs
Clock pulse width high	t_{high}	-	-	12.1	µs
PCI clock rising to EECLK transition	t_{pd1}	-	50	100	ns
PCI clock rising to EEDAT out valid	t_{val1}	-	-	200	ns
EEDAT in valid to EECLK rising	t_{su1}	300	-	-	ns
EEDAT in valid after EECLK rising	t_{hold}	300	-	-	ns

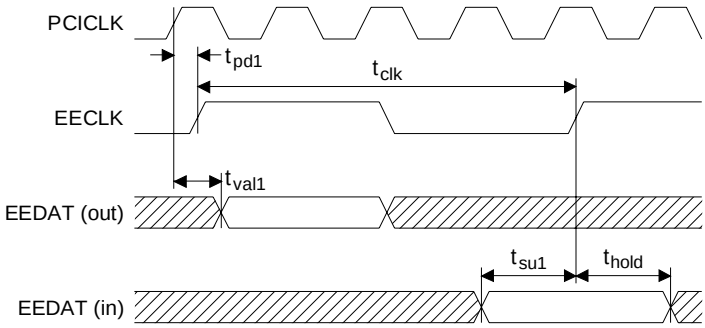


Figure 6. EEPROM Timing Characteristics

MEASURE CONDITION PARAMETERS

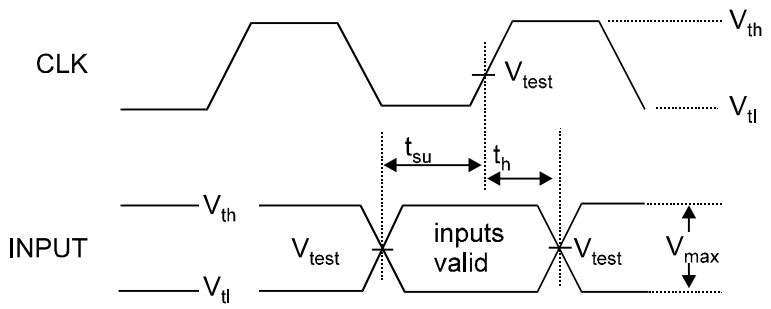


Figure 7. Input Timing Measurement Conditions

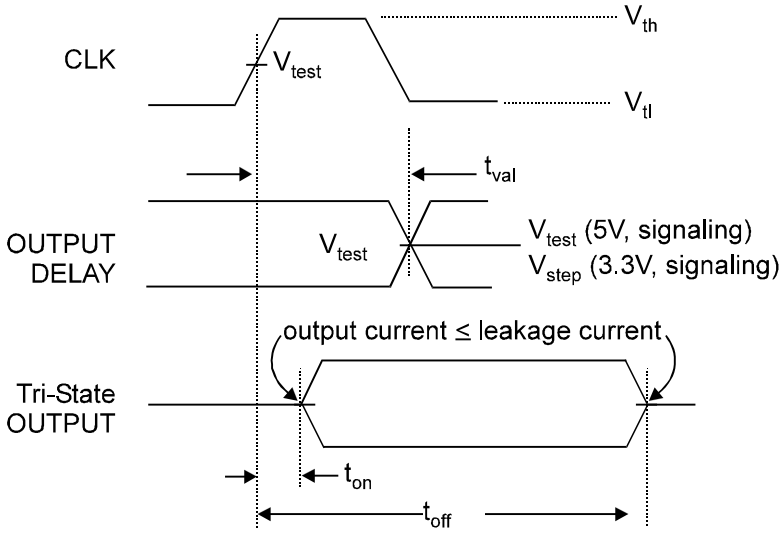


Figure 8. Output Timing Measurement Conditions

OVERVIEW

The CS4610/11 are high performance audio accelerators DSPs for the PCI bus. These devices, combined with application and driver software, provide a complete system solution for cost effective acceleration of Windows® DirectSound®, DirectSound3D®, DirectInput®, ActiveMovie™, MIDI playback via Wavetable Synthesis with reverberation and chorus effects processing, and more.

The CS4610 is a high-performance, full-featured version of the SoundFusion audio accelerator. The CS4611 is a reduced-cost version of the CS4610. The CS4611 has a lower max clock speed and does not support AC-3, Pro Logic, or MPEG-2. Please refer to the OEM Software Reference Manual for more details.

There are three main functional blocks within the CS4610/11: the Stream Processor, the PCI Interface, and the DMA Engine. A block diagram of the CS4610/11 device is shown on the cover page of this data sheet.

The Stream Processor (SP) is a high speed custom Digital Signal Processor (DSP) core designed by Cirrus Logic, Inc. specifically for audio signal processing. This extremely powerful DSP core is capable of running complex algorithms such as Dolby® Digital AC-3™ or MPEG-2 audio decoding for applications such as DVD movie playback or gaming. The Stream Processor is capable of running a number of different signal processing algorithms simultaneously. This high concurrency capability is valuable for applications such as immersive 3D games, which may play a number of DirectSound streams, a number of DirectSound3D streams, and a MIDI music sequence simultaneously.

Separate RAM memories are included on-chip for the SP program code (PROGRAM RAM), parameter data (PARAMETER RAM), and audio sample data (SAMPLE RAM). A small ROM memory (COEFFICIENT ROM) is included to store fixed coefficient data required for the sample rate conversion and audio decompression algorithms.

The RAM-based DSP architecture of the CS4610/11 ensures maximum system flexibility. The software function/feature mix can be adapted to meet the requirements of a variety of different applications, such as DirectX™ games, DVD movie playback, or DOS applications. This RAM-based architecture also provides a means for future system upgrades, allowing the addition of new or upgraded functionality through software updates.

The CS4610/11 provides an extremely efficient bus mastering interface to the PCI bus. The PCI Interface function allows economical burst mode transfers of audio data between host system memory buffers and the CS4610/11 device. Program code and parameter data are also transferred to the CS4610/11 over the PCI Interface.

The CS4610/11 DMA Engine provides dedicated hardware to manage transfer of up to 96 concurrent audio/data streams to and from host memory buffers. The DMA Engine provides hardware scatter-gather support, allowing simple buffer allocation and management. This implementation improves system efficiency by minimizing the number of host interrupts.

The CS4610/11 supports a variety of audio I/O configurations, including direct connection to a CrystalClear CS423xB Codec or to an AC'97 Codec such as the CrystalClear CS4297. The system's flexibility is further enhanced by the inclusion of auxiliary ADC and DAC ports, a bi-directional serial MIDI port, a joystick port, a hardware volume control interface, and a serial data port which allows connection of an optional external EEPROM device.

The block diagram in Figure 9 depicts a motherboard audio subsystem based on the CS4610/11 and the CS423xB. This approach features the proven ISA legacy support of the CS423XB Codec. The CS423xB provides DOS applications with

hardware compatibility for the SoundBlaster Pro™, OPL3™, and MPU-401™ register sets. In this configuration, the CS423xB also provides the system joystick interface. The CS423xB provides all Analog-to-Digital conversion (ADC) and Digital-to-Analog conversion (DAC) functions. Digital audio is transferred between the CS423xB and the CS4610/11 over a proprietary bi-directional serial data link between the two devices. MIDI data from the CS423xB MPU-401 UART is also transferred serially to the CS4610. DOS applications can directly address the CS423xB audio functions on the ISA bus. Windows DirectX audio applications will address the PCI-based CS4610/11 device through Windows DirectX drivers, and the CS423xB is utilized as the external Codec for analog I/O.

A system diagram depicting connection of the CS4610/11 to the CrystalClear CS4297 AC'97 Codec is given in Figure 10. All analog audio inputs and outputs are connected to the AC'97 Codec. Audio data is passed between the AC'97 Codec and the CS4610/11 over the serial AC-Link. The CS4610/11 provides a hardware interface for connection of a joystick and MIDI devices. Legacy audio support under a Windows DOS Box is provided via virtualization of the Sound Blaster, OPL3 FM synthesizer and MPU-401 MIDI Interface registers.

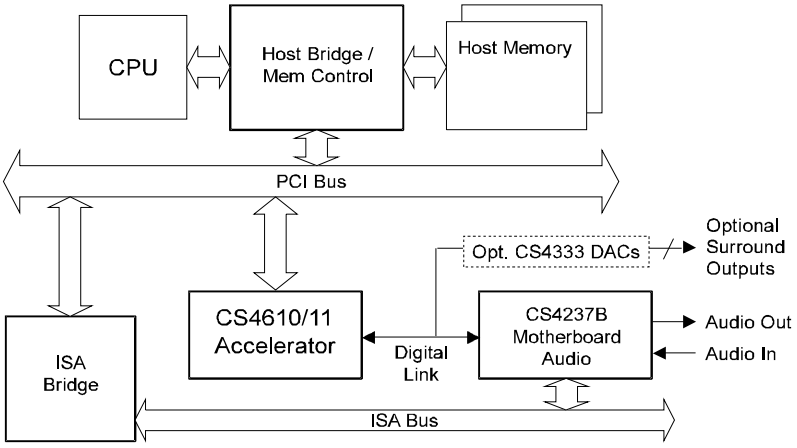


Figure 9. CS4610/11 + CS423XB Motherboard Audio Configuration

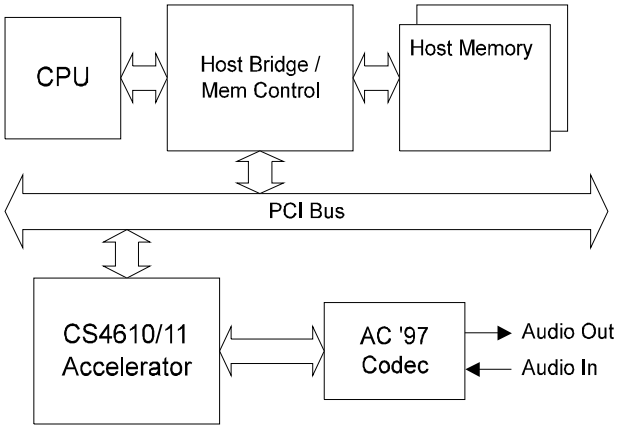


Figure 10. CS4610/11 + AC '97 Codec Configuration

Stream Processor DSP Core

The CS4610/11 Stream Processor (SP) is a custom DSP core design which is optimized for processing and synthesizing digital audio data streams. The SP features a Somewhat Long Instruction Multiple Data (SLIMD) modified dual Harvard architecture. The device uses a 40-bit instruction word and operates on 32-bit data words. The SP includes two Multiply-Accumulate (MAC) blocks and one 16-bit Arithmetic and Logic Unit (ALU). The SP core is conservatively rated at 300 Million Instructions per second (300 MIPS) when running at a 100 MHz internal clock speed (CS4611 runs at 80 MHz). The MAC units perform 20-bit by 16-bit multiplies and have 40-bit accumulators, providing higher quality than typical 16-bit DSP architectures.

PLL and Clock Control

The CS4610/11 includes a programmable Phase Locked Loop (PLL) circuit which is utilized to generate the high frequency internal SP clock from a lower frequency input clock. The input to the PLL may be from the CS4610/11 crystal oscillator circuit, the serial port clock (SCLK) or the PCI bus clock (PCICLK). The PCICLK is used as an input to the PLL for test modes only. The CS4610/11 Clock Control circuitry allows gating of clocks to various internal functional blocks to conserve power during power conservation modes, as well as during normal modes of operation when no tasks are being executed.

Host Interface

The CS4610/11 host interface is comprised of two separate interface blocks which are memory mapped into host address space. The CS4610/11 interface blocks can be located anywhere in the host 32-bit physical address space. The interface block locations are defined by the addresses programmed into the two Base Address Registers in the CS4610/11 PCI Configuration Space. These base addresses are normally set up by the system's Plug and Play BIOS. The first interface block (located by Base Address 0) is a 4 KB register block containing general purpose configuration, control, and status registers for the device. The second interface block (located by Base Address 1) is a 1 MB block which maps all of the CS4610/11 internal RAM memories (SP Program RAM, Parameter RAM, and Sample RAM), along with the SP debug registers, into host memory space. This allows the host to directly peek and poke RAM locations on the device. The relationship between the Base Address Registers in the CS4610/11 PCI Configuration Space and the host memory map is depicted in Figure 11.

CS4610/11 PCI Interface

The CS4610/11 provides a bus mastering PCI bus interface which complies with the PCI Local Bus Specification version 2.1.

PCI bus transactions

As a target of a PCI bus transaction, the CS4610/11 supports the Memory Read (from internal registers or memory), Memory Write (to internal registers or memory), Configuration Read (from CS4610/11 configuration registers), Configuration Write (to CS4610/11 configuration registers), Memory Read Multiple (aliased to Memory Read), Memory Read Line (aliased to Memory Read), and the Memory Write and Invalidate (aliased to Memory Write) transfer cycles. The I/O Read, I/O Write, Interrupt Acknowledge, Special Cycles, and Dual Address Cycle transactions are not supported.

As Bus Master, the CS4610/11 generates the Memory Read Multiple and Memory Write transactions. The Memory Read, Configuration Read, Configuration Write, Memory Read Line, Memory Write and Invalidate, I/O Read, I/O Write, Interrupt Acknowledge, Special Cycles, and Dual Address Cycle transactions are not generated.

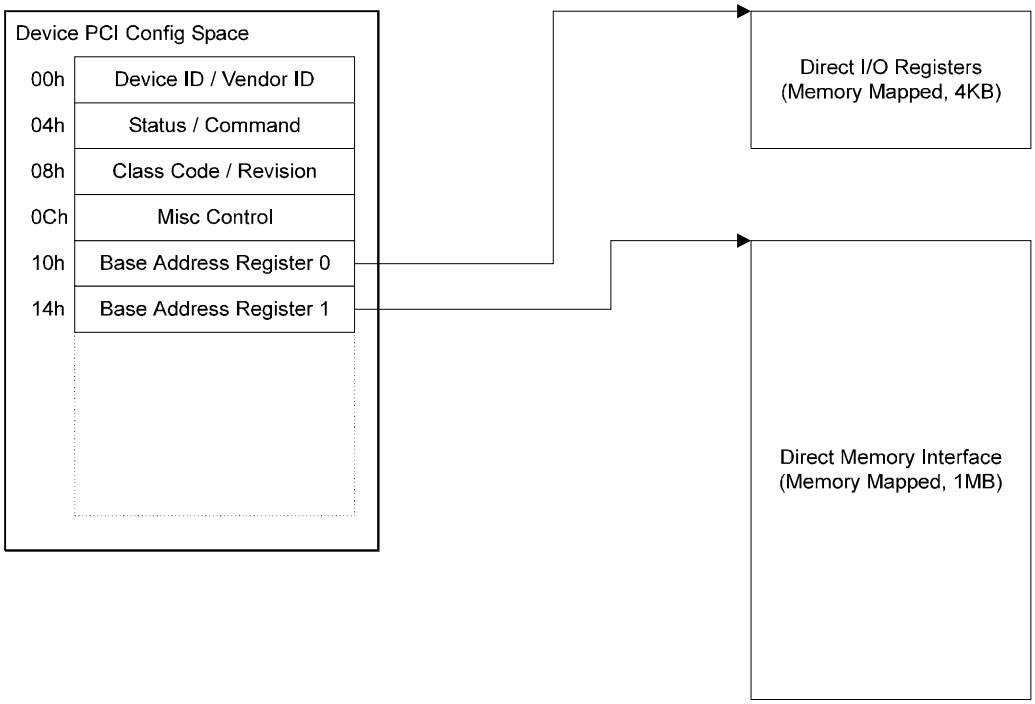


Figure 11. CS4610/11 Host Interface Base Address Registers

Initiator	Target	Type	PCI Dir
Host	Registers (BA0)	Mem Write	In
Host	Registers (BA0)	Mem Read	Out
Host	Memories (BA1)	Mem Write	In
Host	Memories (BA1)	Mem Read	Out
Host	Config Space 1	Config Write	In
Host	Config Space 1	Config Read	Out
DMA	Host System	Mem Write	Out
DMA	Host System	Mem Read	In

Table 1. CS4610/11 PCI Interface Transaction Summary

The PCI bus transactions supported by the CS4610/11 device are summarized in Table 1. Note that no Target Abort conditions are signalled by the device. Byte, Word, and Doubleword transfers are supported for Configuration Space accesses. Only Doubleword transfers are supported for Register or Memory area accesses. Bursting is not supported for host-initiated transfers to/from the CS4610/11 internal register space, RAM memory space, or PCI configuration space (disconnect after first phase of transaction is completed).

Configuration Space

The content and format of the primary PCI Configuration Space for the CS4610/11 device is given in Table 1.

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Device ID: R/O, 6001h 6XXXh range for Crystal and CrystalClear		Vendor ID: R/O, 1013h (Cirrus Logic's PCI ID)		00h
Status Register, bits 15-0: Bit 15 Detected Parity Error: Error Bit Bit 14 Signalled SERR: Error Bit Bit 13 Received Master Abort: Error Bit Bit 12 Received Target Abort: Error Bit Bit 11 Signalled Target Abort: Error Bit Bit 10-9 DEVSEL Timing: R/O, 01b (medium) Bit 8 Data Parity Error Detected: Error Bit Bit 7 Fast Back to Back Capable: R/O 0 Bit 6-0UDF, 66MHz, Reserved: R/O 0000000 Reset Status State: 0200h Write of 1 to any error bit position clears it.		Command Register, bits 15-0: Bit 15-10: Reserved, R/O 0 Bit 9 Fast B2B Enable: R/O 0 Bit 8 SERR Enable: R/W, default 0 Bit 7 Wait Control: R/O 0 Bit 6 Parity Error Response: R/W, default 0 Bit 5 VGA Palette Snoop: R/O 0 Bit 4 MWI Enable: R/O 0 Bit 3 Special Cycles: R/O 0 Bit 2 Bus Master Enable: R/W, default 0 Bit 1 Memory Space Enable: R/W, default 0 Bit 0 IO Space Enable: R/O 0		04h
Class Code: R/O 040100h (Note: change from 80h) Class 04h (multimedia device), Sub-class 01h (audio), Interface 00h			Revision ID: R/O 01h	08h
BIST: R/O 0	Header Type: Bit 7: R/O 0 Bit 6-0: R/O 0 (type 0)	Latency Timer: Bit 7-3: R/W,default 0 Bit 2-0: R/O 0	Cache Line Size: R/O 0	0Ch
Base Address Register 0 Device Control Register space, memory mapped. 4KB size Bit 31-12: R/W, default 0. Compare address for register space accesses Bit 11 - 4: R/O 0, specifies 4KB size Bit 3: R/O 0, Not Prefetchable (Cacheable) Bit 2-1: R/O 00, Location Type - Anywhere in 32 bit address space Bit 0: R/O 0, Memory space indicator				10h
Base Address Register 1 Device Memory Array mapped into host system memory space, 1MB size Bit 31-20: R/W, default 0. Compare address for memory array accesses Bit 19 - 4: R/O 0, specifies 1MB size Bit 3: R/O 0, Not Prefetchable (Cacheable) Bit 2-1: R/O 00, Location Type - Anywhere in 32 bit address space Bit 0: R/O 0, Memory space indicator				14h
Base Address Register 2: R/O 00000000h, Unused				18h
Base Address Register 3: R/O 00000000h, Unused				1Ch
Base Address Register 4: R/O 00000000h, Unused				20h
Base Address Register 5: R/O 00000000h, Unused				24h
Cardbus CIS Pointer: R/O 00000000h, Unused				28h
Subsystem ID R/O 0000h if EXTEE not present, otherwise R/W, loaded from EEPROM		Subsystem Vendor ID R/O 0000h if EXTEE not present, otherwise R/W, loaded from EEPROM		2Ch

Table 1. CS4610/11 PCI Configuration Space 1

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Expansion ROM Base Address: R/O 00000000h, Unused				30h
Reserved: R/O 00000000h				34h
Reserved: R/O 00000000h				38h
Max_Lat: R/O 18h 24 x 0.25uS = 6 uS	Min_Gnt: R/O 04h 4 x 0.25uS = 1uS	Interrupt Pin: R/O 01h, INTA used	Interrupt Line: R/W, default 0	3Ch

Table 1. CS4610/11 PCI Configuration Space 1 *(Continued)*

Subsystem Vendor ID Fields

The Subsystem ID and Subsystem Vendor ID fields in the CS4610/11 PCI Configuration Space default to value 0000h unless an external EEPROM device is detected or unless the host has written to the appropriate internal register to program the values.

CS4610/11 Interrupt Signal

The CS4610/11 PCI Interface includes an interrupt controller function which receives interrupt requests from multiple sources within the CS4610/11 device, and presents a single interrupt line (INTA) to the host system. Interrupt control registers in the CS4610/11 provide the host interrupt service routine with the ability to identify the source of the interrupt and to clear the interrupt sources. In the CS4610/11, the single external interrupt is expanded by the use of "virtual channels". Each data stream which is read from or written to a modulor buffer is assigned a virtual channel number. This virtual channel number is signalled by the DMA subsystem anytime the associated modulo buffer pointer passes the mid-point or wraps around. Virtual channels are also used for message passing between the CS4610/11 and the host.

Serial Port Configurations

The CS4610/11 provides a flexible Serial Audio Interface which allows connection to external Analog-to-Digital Converters (ADCs), Digital-to-Analog Converters (DACs) or Codecs (combined ADC and DAC functions) in several different configurations. The CS4610/11 serial audio interface includes a primary input/output port with dedicated serial data pins (SDIN, SDOUT), two auxiliary audio output ports (SDO2, SDO3) which share pins with the joystick interface button input functions, and one auxiliary audio input port (SDIN2). Each of these digital audio input and output pins carry two channels of audio data. These two channels may comprise the left and right channels of a stereo audio signal, or they may be two independent monaural audio signals.

Each digital audio channel is internally buffered through a 16 sample x 20-bit FIFO. The data format for the serial digital audio ports varies depending on the configuration. The primary configurations supported include a CS4610/11 plus CS423xB configuration for motherboard audio, a CS4610/11 plus CS423xB configuration with full 5.1 channel output capability, and an AC'97 controller configuration (CS4610/11 plus an AC'97 Codec).

CS4610/11 + CS423xB Motherboard Audio Accelerator

A system block diagram for the CS4610/11 plus CS423xB configuration is given in Figure 9. This configuration utilizes a proprietary bi-directional digital audio link between the CS4610/11 and the CS423xB. The connection between these devices is depicted in Figure 12.

In the CS4610/11 plus CS423xB configuration, the CS423xB is the serial port timing master. The se-

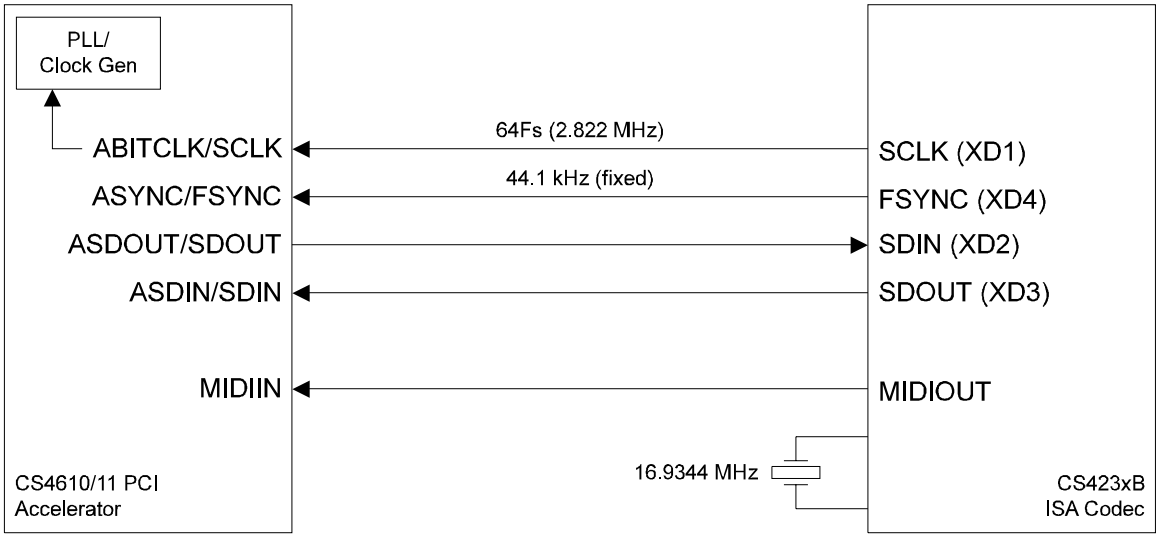


Figure 12. CS4610/CS423XB Connection Diagram

rial port runs at a fixed 44.1 kHz sampling rate, and the 2.822 MHz SCLK output from the CS423xB is selected as the CS4610/11 PLL clock generator input.

Note that in this configuration the SDIN signal carries two stereo streams from the CS423xB to the CS4610/11; the CS423xB ADC data and the CS423xB final digital mix output data. The SDOUT signal carries the CS4610/11 final output to the CS423xB digital mixer. SDIN and SDOUT transitions occur on rising edges of SCLK (SDIN is sampled on falling edges of SCLK). The data is transmitted in left-justified format, MSB first, 16-bit data, with 32 clock cycles for each phase of the FSYNC signal. FSYNC transitions occur on rising edges of SCLK, the FSYNC high phase indicates left channel data on SDIN and SDOUT while the FSYNC low phase indicates right channel data. The SDOUT signal carries 16 bits of data followed by 16 bits of zero pad for each channel (left and right). The SDIN signal carries 16 bits of ADC data followed by 16 bits of DAC data for each channel (left and right). The serial port clock and data timing relationship for this configuration is indicated Figure 13. The clock and data signal functions for this configuration are summarized in Table 3.

Motherboard Configuration with 5.1 channel output capability (CS4610 only)

This configuration is the same as the CS4610 plus CS423xB motherboard accelerator configuration with the addition of two Crystal™ CS4333 Stereo DACs to expand the audio output capability to six channels. This expanded output capability is useful for applications where discrete 5.1 channel output is desired for Dolby AC-3 audio programs. The connection diagram for the additional CS4333 DACs is given in Figure 14. The CS4333 DACs share the SCLK output from the CS423xB with the CS4610. The CS4333 DACs also receive a 16.9344 MHz MCLK signal from the CS423xB. Note that the CS423xB MCLK output has limited drive strength and should be buffered in this application. The LRCLK framing clock and the SDO2/SDO3 digital audio outputs are provided from the CS4610. The SDO2 and SDO3 transitions occur on falling edges of SCLK (the primary output SDOUT transitions on rising edges of SCLK). LRCLK transitions occur on falling edges of SCLK, with the LRCLK high phase indicating left channel data present on SDO2/SDO3. SDO2/SDO3 data is right justified, with 16 bits of zero pad followed by 16-bits of data, transmitted

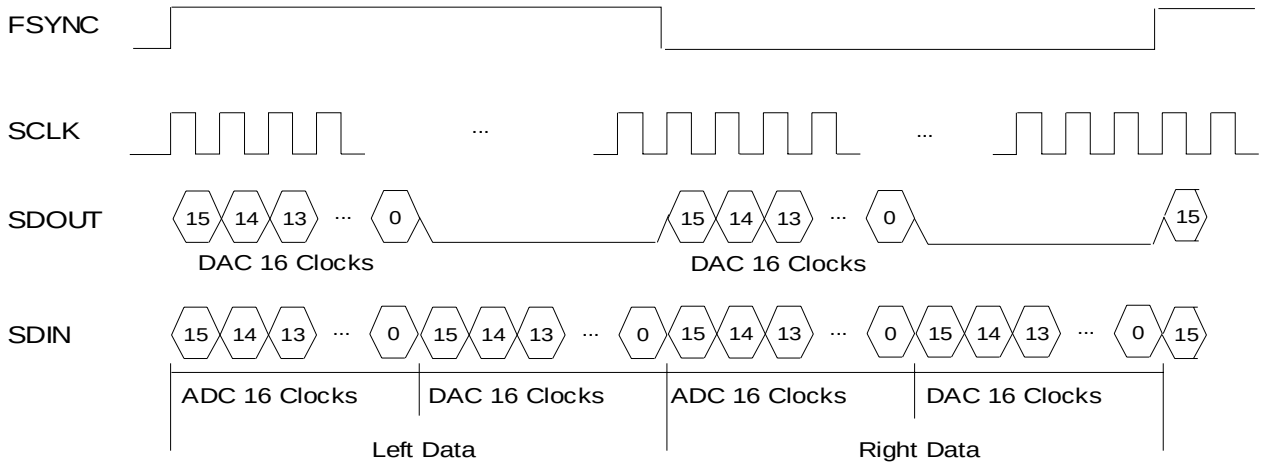


Figure 13. Serial Audio Port Format for CS4610/11 + CS423XB Configuration

Pin Name	Direction	Functional Description
SCLK	Input	Main timing driver for digital audio link, both edges used internally for timing. Also functions as the source to the PLL for internal clock generation.
FSYNC	Input	Framing signal for digital audio link, high time indicates left channel data and low time indicates right channel data. Frame should be sampled on the falling edge of the SCLK input.
SDOUT	Output	Primary output port serial data pin. This data is the CS4610/11 output stream going to the CS423XB digital mixer. The serial data on this pin should transition off of the rising edge of the SCLK input.
SDIN	Input	Primary input port serial data pin. This data contains both CS423XB ADC data and the CS423XB final digital mix output data. The serial data on this pin should be sampled on the falling edge of the SCLK input.

Table 3. Serial Audio Port Signal Summary for CS4610/11 + CS423XB Configuration

MSB first. There are 64 SCLKs per LRCLK, and MCLK runs at 384× the frame rate. The serial port clock and data timing relationship for this configuration is indicated Figure 15. The clock and data signal functions for this configuration are summarized in Table 4.

AC'97 Controller Configuration

In this configuration the CS4610/11 functions as an AC'97 controller. The CS4610/11 communicates with an AC'97 Codec, such as the CrystalClear CS4297, over the AC-link as specified in the Intel® Audio Codec ' 97 Specification version 1.0.3. A block diagram for the AC'97 Controller Configuration is given in Figure 10. The signal connections between the CS4610/11 and the AC'97 Codec are indicated in Figure 16. In this configuration, the AC'97 Codec is the timing master for the digital audio link. The CS4610/11 ADSOUT output supports data transmission on all 10 possible sample slots (output slots 3 - 12). The CS4610/11 ASDIN input supports receiving of audio sample data on 6 input sample slots (input slots 3 - 8). The SDO2,

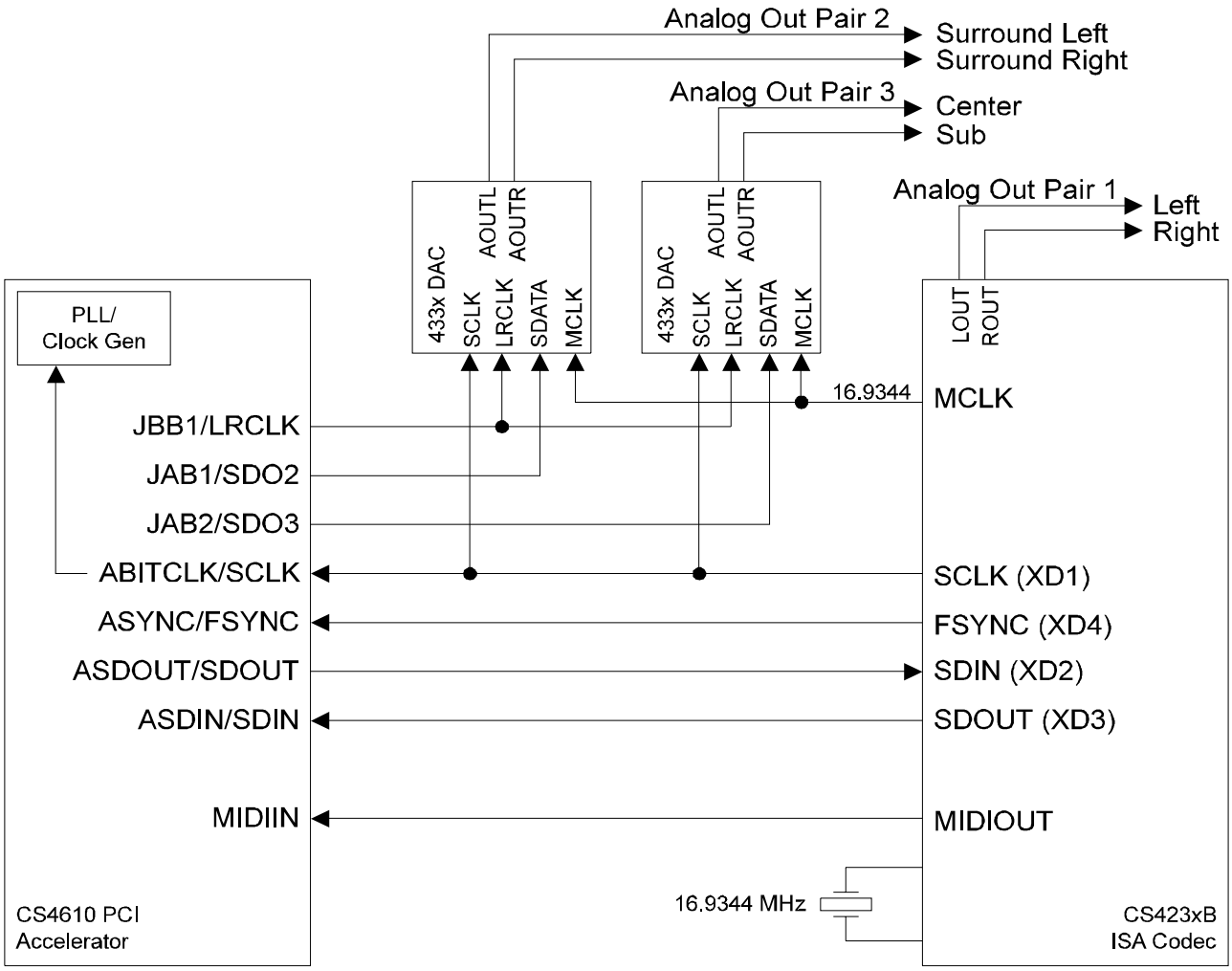


Figure 14. CS4610 + CS423XB Expanded 6-Channel Output Configuration

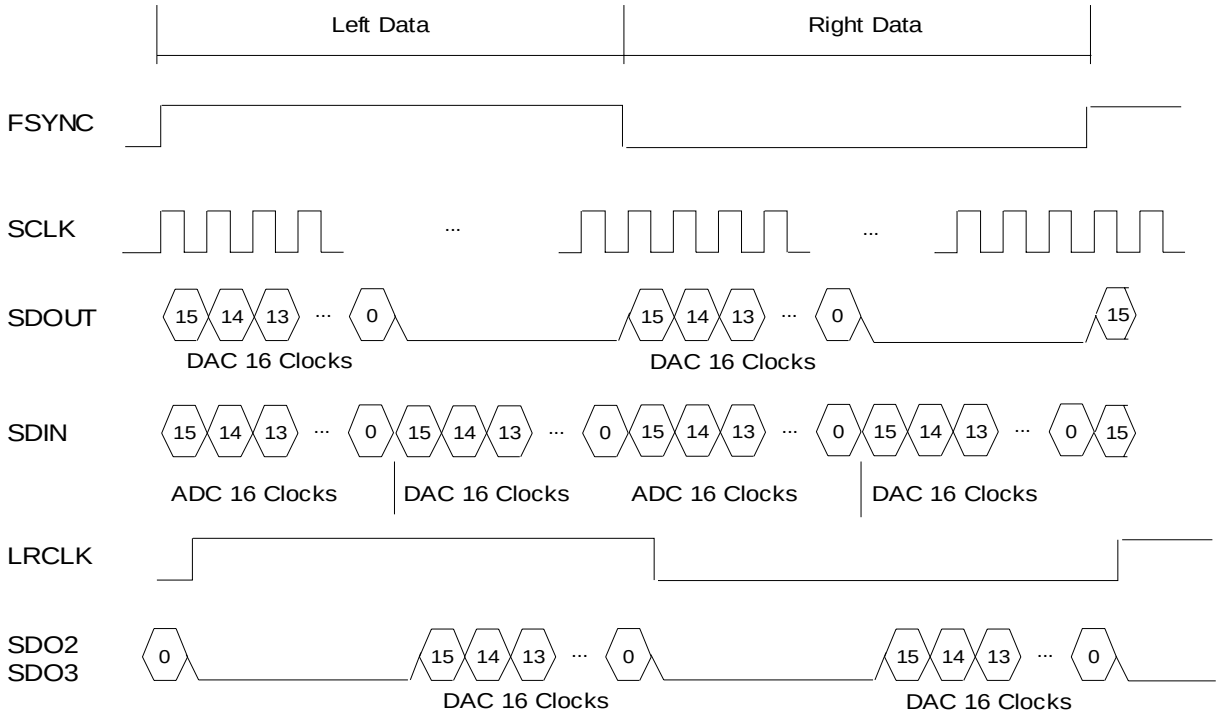


Figure 15. Serial Audio Port Format for CS4610 + CS423XB Expanded Output Configuration.

Pin Name	Direction	Functional Description
SCLK	Input	Main timing driver for digital audio link, both edges used internally for timing. Also functions as the source to the PLL for internal clock generation.
FSYNC	Input	Framing signal for digital audio link, high time indicates left channel data and low time indicates right channel data. Frame should be sampled on the falling edge of the SCLK input.
SDOUT	Output	Primary output port serial data pin. This data is the CS4610 output stream going to the CS423XB digital mixer. The serial data on this pin should transition off of the rising edge of the SCLK input.
SDIN	Input	Primary input port serial data pin. This data contains both CS423XB ADC data and the CS423XB final digital mix output data. The serial data on this pin should be sampled on the falling edge of the SCLK input.
LRCLK	Output	Framing signal for external 4333 DACs, high time indicates left channel data and low time indicates right channel data. This pin should transition off of the falling edge of the SCLK input.
SDO2, SDO3	Output	Second and third output port serial data pins. These output streams are the expanded output channels beyond the CS423XB left / right pair. The serial data on these pins should transition off of the falling edge of the SCLK input. Note that this is a DIFFERENT edge than the one for the SDOUT pin.

Table 4. Serial Audio Port Signal Summary for CS4610 + CS423XB Expanded Output Configuration

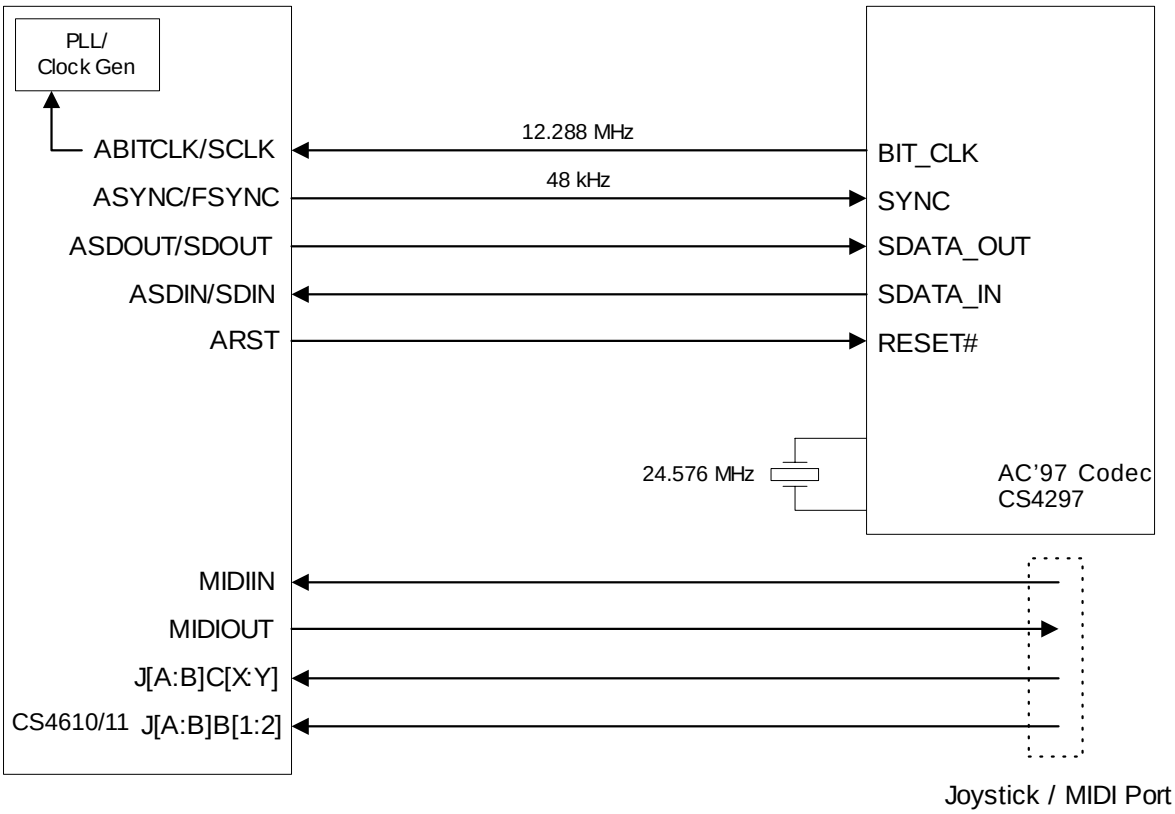


Figure 16. CS4610/11 - AC '97 Codec Connection Diagram

SDO3 serial outputs and the SDIN2 serial input are not supported in this configuration.

MIDI Port

In the AC'97 controller configuration, the CS4610/11 provides a bi-directional MIDI interface to allow connection of external MIDI devices. The CS4610/11 MIDI interface includes 16-byte FIFOs for the MIDI transmit and receive paths.

Joystick Port

In the AC'97 controller configuration, the CS4610/11 provides a joystick port. The CS4610/11 joystick port provides four "coordinate" channels and four "button" channels of input capability. The coordinate channels provide joystick positional information to the host, and the button channels provide user button event information. The joystick interface is capable of operating in the traditional "polled" mode, but also provides a "hardware accelerated" mode of operation wherein internal counters are provided to assist the host with coordinate position determination.

EEPROM Configuration Interface

The CS4610/11 EEPROM configuration interface allows the connection of an optional external EEPROM device to provide power-up configuration information. The external EEPROM is not required for proper operation of the CS4610. However, in some applications power-up configuration settings other than the CS4610/11 device default values may be required to support specific Operating System compatibility requirements (the CS4610/11 default is the CS4610/11 + CS423XB configuration).

After a hardware reset, an internal state machine in the CS4610/11 will automatically detect the presence of an external EEPROM device and load the Subsystem ID and Subsystem Vendor ID fields, along with two bytes of general configuration information, into internal registers. At power-up, the CS4610/11 will attempt to read from the external device, and will check the data received from the device for a valid signature header. If the header data is invalid, the data transfer is aborted. After power-up, the host can read or write from/to the EEPROM device by accessing ("bit-banging") specific registers in the CS4610/11.

The two wire interface for the optional external EEPROM device is depicted in Figure 17. During data transfers, the data line (EEDAT) can change state only while the clock signal (EECLK) is low. A state change of the data line while the clock signal is high indicates a start or stop condition to the EEPROM device.

The EEPROM device read access sequence is shown in the Figure 18. The timing follows that of a random read sequence. The CS4610/11 first performs a "dummy" write operation, generating a start condition followed by the slave device address and the byte address of zero. The slave address is made up of a device identifier (0xA) and a bank select (bits A2-A0). The bank select bits select among eight 256 byte blocks. The bank select bits may be used to select among multiple 256 byte blocks within a single device. i.e. a 1 K byte memory may be comprised of a single 1 K byte EEPROM with four 256 byte banks. The CS4610/11 always begins access at byte address zero and continues access a byte at a time. The byte address automatically increments by one until a stop condition is detected.

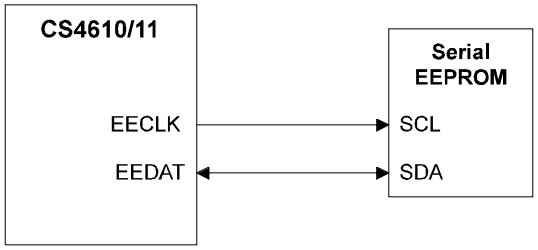


Figure 17. External EEPROM Connection

General Purpose I/O Pins

Many of the CS4610/11 signal pins are internally multiplexed to serve different functions depending on the environment in which the device is being used. Several of the CS4610/11 signal pins may be used as general purpose I/O pins when not required for other specific functions in a given application.

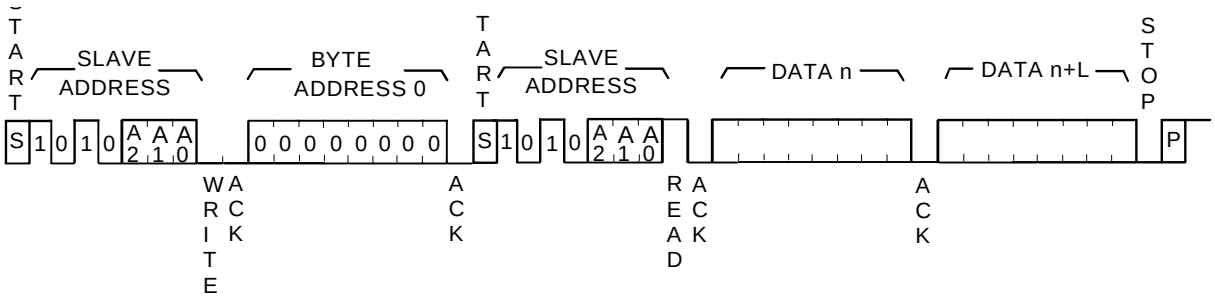
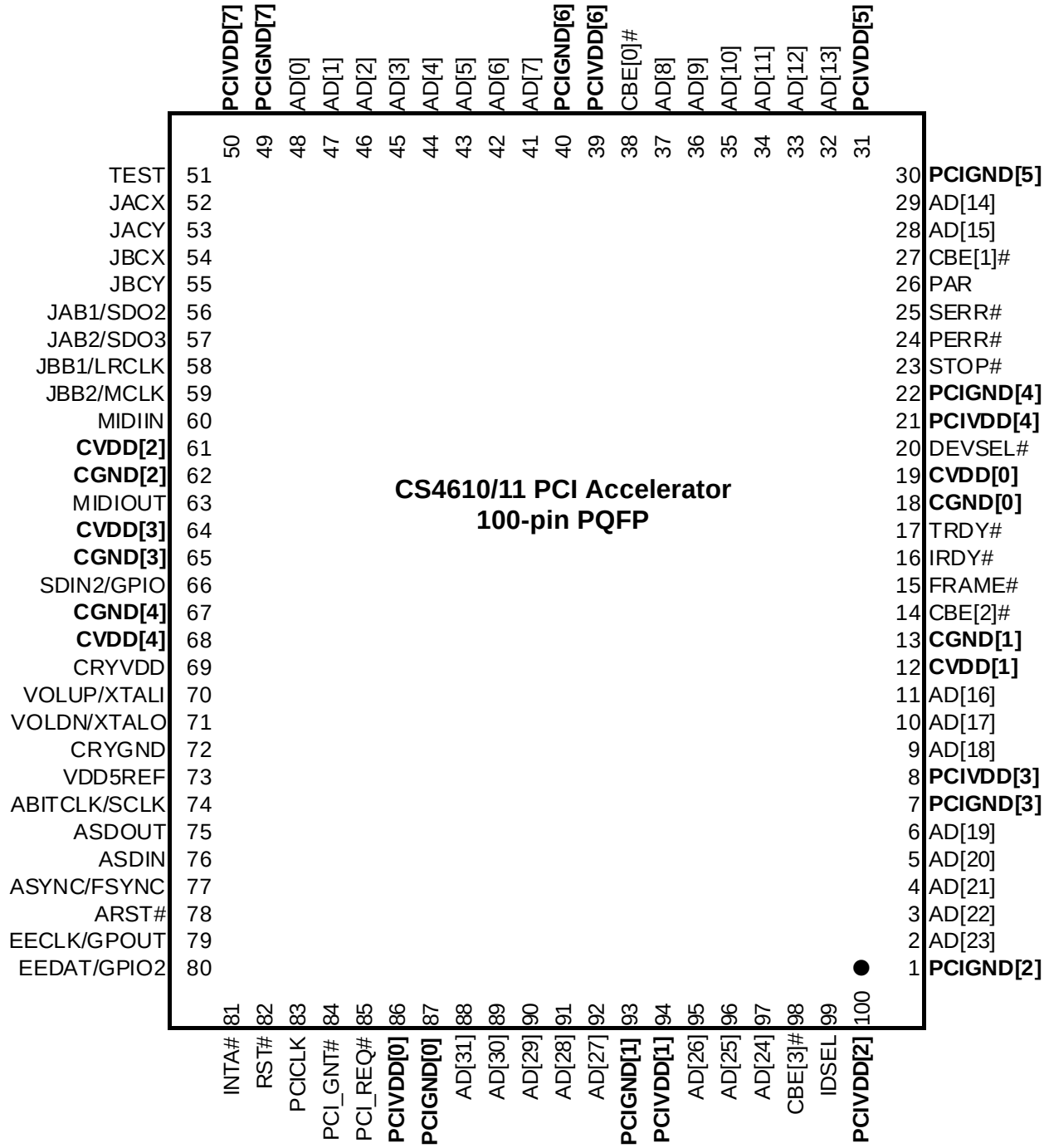


Figure 18. External EEPROM Read Access Sequence

PIN OUT

Physical Pin Placement



Pin Descriptions

PCI Interface

AD[31:0] : pins 88-92, 95-97, 2-6, 9-11, 28-29, 32-37, 41-48

Address / Data Bus

Input / Output

These pins form the multiplexed address / data bus for the PCI interface.

C_BE[3:0]# : pins 98, 14, 27

Command Type / Byte Enables

Input / Output

These four pins are the multiplexed command / byte enables for the PCI interface. During the address phase of a transaction, these pins indicate cycle type. During the data phases of a transaction, active low byte enable information for the current data phase is indicated. These pins are inputs during slave operation and they are outputs during bus mastering operation.

PAR : pin 26

Parity

Input / Output, Active High

The Parity pin indicates even parity across AD[31:0] and C_BE[3:0] for both address and data phases. The signal is delayed one PCI clock from either the address or data phase for which parity is generated.

FRAME# : pin 15

Cycle Frame

Input / Output, Active Low

FRAME# is driven by the current PCI bus master to indicate the beginning and duration of a transaction.

IRDY# : pin 16

Initiator Ready

Input / Output, Active Low

IRDY is driven by the current PCI bus master to indicate that as the initiator it is ready to transmit or receive data (complete the current data phase).

TRDY# : pin 17

Target Ready

Input / Output, Active Low

TRDY# is driven by the current PCI bus target to indicate that as the target device it is ready to transmit or receive data (complete the current data phase).

STOP# : pin 23

Transaction Stop

Input / Output, Active Low

STOP# is driven active by the current PCI bus target to indicate a request to the master to stop the current transaction.

IDSEL : pin 99

Initialize Device Select

Input, Active High

IDSEL is used as a chip select during PCI configuration read and write cycles.

DEVSEL# : pin 20

Device Select

Input / Output, Active Low

DEVSEL# is driven by the PCI bus target device to indicate that it has decoded the address of the current transaction as its own chip select range.

PCI_REQ# : pin 85

Master Request

Tri-state Output, Active Low

PCI_REQ# indicates to the system arbiter that this device is requesting access to the PCI bus. This pin must be tri-stated when RST# is active.

PCI_GNT# : pin 84

Master Grant

Input, Active Low

PCI_GNT# is driven by the system arbiter to indicate to the device that the PCI bus has been granted.

PERR# : pin 24

Parity Error

Input / Output, Active Low

PERR# is used for reporting data parity errors on the PCI bus.

SERR# : pin 25

System Error

Open Drain, Active Low

SERR# is used for reporting address parity errors and other catastrophic system errors. (Warning: may generate processor NMI.)

INTA# : pin 81

Host Interrupt A (for SP)

Open Drain, Active Low

INTA# is the level triggered interrupt pin dedicated to servicing internal device interrupt sources.

PCI_CLK : pin 83

PCI Bus Clock

Clock Input, Rising Edge

PCI_CLK is the PCI bus clock for timing all PCI transactions. All PCI synchronous signals are generated and sampled relative to the rising edge of this clock.

RST# : pin 82

PCI Device Reset

Input, Active Low

RST# is the PCI bus master reset.

VDD5REF : pin 73

Clean 5V for Pseudo Supply

Power

VDD5REF is the power connection pin for the 5 V PCI pseudo supply for the PCI bus drivers.

PCIVDD[7:0] : pins 50, 39, 31, 21, 8, 100, 94, 86

PCI Driver Power

Power

PCIVDD pins are the PCI driver power supply pins.

PCIGND[7:0] : pins 49, 40, 30, 22, 7, 1, 93, 87

PCI Driver Ground

Ground

PCIGND pins are the PCI driver ground reference pins.

External Interface Pins

TEST : pin 51

Test Mode Strap

Input, Active High

This pin is sampled at reset for test mode entry. If it is high at reset, test mode is enabled. This pin should normally be pulled to ground in a production design.

EEDAT/GPIO2 : pin 80

External EEPROM Data / General Purpose IO Pin 2

Input / Output, Open Drain

Data line for external serial EEPROM containing device configuration data. In designs without EEPROM requirements, this pin can be used as a general purpose input or open drain output.

EECLK/GPOUT : pin 79

External EEPROM Clock / General Purpose Output Pin

Output, Active High

Clock line for external serial EEPROM containing device configuration data. In designs without EEPROM requirements, this pin can be used as a general purpose output pin.

SDIN2/GPIO : pin 66

Serial Data Input 2 / General Purpose IO Pin

Input / Output, Multiplexed Function Pin

This dual function pin defaults as a general purpose I/O pin. In non-AC'97 system configurations, this pin can function as a second stereo digital data input pin if enabled.

VOLUP/XTALI : pin 20

Volume Up Button / Crystal Input

Input, Active Low or Analog Input

This dual function pin is either the volume up button control input or the crystal oscillator input pin, depending on system configuration. This pin may also be used as a general purpose input if its primary function is not needed.

VOLDN/XTALO pin 71

Volume Down Button / Crystal Output

Input, Active Low or Analog Output

This dual function pin is either the volume down button control input or the crystal oscillator output pin, depending on system configuration. This pin may also be used as a general purpose input if its primary function is not needed.

Clock / Miscellaneous

CRYVDD : pin 69

Crystal / PLL Power

Power

Power pin for crystal oscillator and internal phase locked loop.

CRYGND : pin 72

Crystal / PLL Ground

Ground

Ground pin for crystal oscillator and internal phase locked loop.

J[A:B]C[X:Y] : pins 52, 53, 54, 55

Joystick Coordinate Inputs

Analog Input

These pins are the 4 axis analog inputs for the joystick port. These pins may also be used as a general purpose inputs or open drain outputs if their primary function is not needed.

JAB1/SDO2 : pin 56

Joystick A Button 1

Input / Output, Multiplexed Function Pin

This dual function pin defaults as JAB1 (button input pin for joystick A, button 1). In non-AC'97 system configurations, this pin can function as a second stereo digital data output pin if enabled. This pin can also be used as a general purpose polled input if a second data output stream is not required.

JAB2/SDO3 : pin 57

Joystick A Button 2

Input / Output, Multiplexed Function Pin

This dual function pin defaults as JAB2 (button input pin for joystick A, button 2). In non-AC'97 system configurations, this pin can function as a third stereo digital data output pin if enabled. This pin can also be used as a general purpose polled input if a third data output stream is not required.

JBB1/LRCLK : pin 58

Joystick B Button 1

Input / Output, Multiplexed Function Pin

This dual function pin defaults as JBB1 (button input pin for joystick B, button 1). In non-AC'97 system configurations, this pin can function as an alternate framing clock output pin for SDO2 and SDO3. This pin can also be used as a general purpose polled input if alternate data output streams are not required.

JBB2/MCLK : pin 59

Joystick B Button 2

Input / Output, Multiplexed Function Pin

This dual function pin defaults as JBB2 (button input pin for joystick B, button 2). In non-AC'97 system configurations, this pin can function as a master (256x sample rate) output clock if enabled. This pin can also be used as a general purpose polled input if alternate data output streams are not required.

MIDIIN : pin 60

MIDI Data Input

Input, Active High

This is the serial input pin for the internal MIDI port.

MIDIOUT : pin 63

MIDI Data Output

Output, Active High

This is the serial output pin for the internal MIDI port.

CVDD[4:0] : pins 68, 64, 61, 12, 19

Core Power

Power

Core / Stream Processor power pins.

CGND[4:0] : pins 67, 65, 62, 13, 18

Core Ground

Ground

Core / Stream Processor ground reference pins.

Serial Codec Interface

ABITCLK/SCLK : pin 74

AC'97 Bit Rate Clock / Serial Audio Data Clock

Input / Output

Master timing clock for serial audio data. In AC'97 configurations, this pin is an input which drives the timing for the AC'97 interface, along with providing the source clock for the PLL. In CS423XB digital link configurations, this pin is an input for the SCLK from the CS423XB DSP port. In external DAC configurations, this pin is an output, providing the serial bit clock.

ASYNC/FSYNC : pin 77

AC'97 Frame Sync / Serial Audio Out Framing

Input / Output

Framing clock for serial audio data. In AC'97 configurations, this pin is an output which indicates the framing for the AC'97 link. In CS423XB digital link configurations, this pin is an input for the FSYNC from the CS423XB DSP port. In external DAC configurations, this pin is an output, providing the LRCLK frame clock.

ASDOUT/SDOUT : pin 75

AC'97 Data Out / Serial Audio Out Data

Output, Active High

Serial audio output data.

ASDIN/SDIN : pin 76

AC'97 Data In / Serial Audio Input Data

Input, Active High

Serial audio input data.

ARST# : pin 78

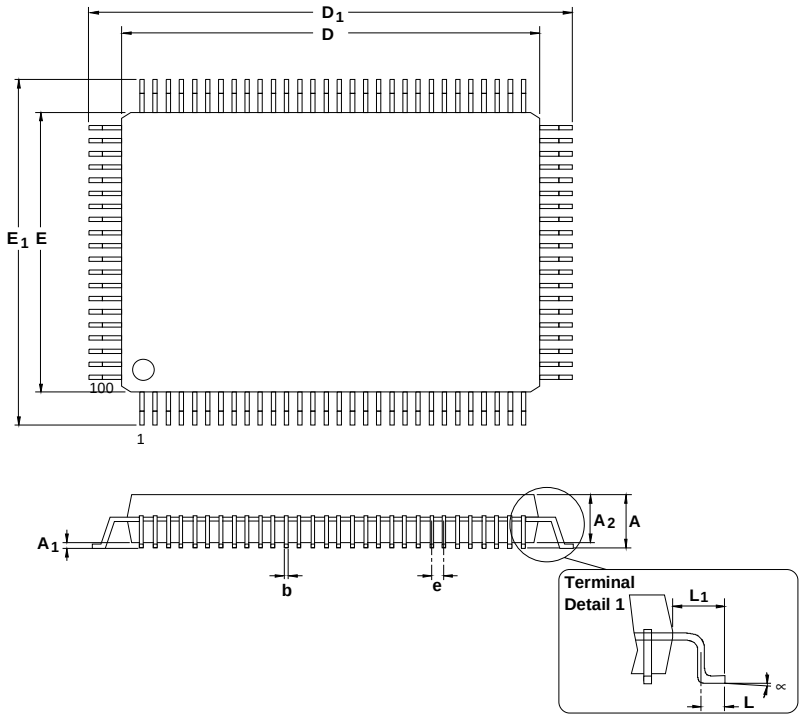
AC'97 Reset Pin

Output, Active Low

AC'97 link reset pin. This pin also functions as a general purpose reset output in non-AC'97 configurations. This pin will follow the PCI RST# pin 82 to ground, but must be forced high by software.

MECHANICAL DRAWING

100-pin PQFP



100 Lead PQFP						
	MILLIMETERS			INCHES		
DIM	MIN	NOM.	MAX	MIN	NOM.	MAX
A	2.82	3.07	3.32	0.111	0.121	0.131
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
D	19.90	20.00	20.10	0.783	0.787	0.791
D_1	23.00	23.20	23.40	0.905	0.913	0.921
E	13.90	14.00	14.10	0.547	0.551	0.555
E_1	17.00	17.20	17.40	0.669	0.677	0.685
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	- - -	1.60	- - -	- - -	0.063	- - -
N		100			100	
e	- - -	0.65	- - -	- - -	0.026	- - -
b	0.20	0.30	0.40	0.008	0.012	0.016
∝	0°	- - -	12°	0°	- - -	12°