BELL TELEPHONE LABORATORIES
INCORPORATED

SUBJECT: PDP-7 and PDP-9 to 201A Data Phone Interface

DATE: May 18, 1967

FROM: P. E. Rosenfeld

MEMORANDUM FOR FILE

INTRODUCTION

An interface has been designed to connect a DEC PDP-7 or PDP-9 computer to a 201 Data Phone. The 201 may be run in either half or full duplex modes at either 2000 or 2400 bits per second. The interface accepts a 7-bit parallel word from the computer, adds an eighth bit for parity, and transmits it serially. It receives serial eight bit characters, checks and strips the parity bit, and hands a 7-bit parallel word to the computer.. The interface can be modified for other bit rates and word lengths. The interface has provisions for synchronizing itself to the incoming data stream. It can either be left in the receiving state, or transmitting 1's. Double buffering is provided on both the receiver and transmitter.

PROGRAMMING

The following IOT instructions are used to operate the Data Phone interface:

DPØN 704701 Data Phone ON

Causes the interface to set the 201A data phone to the Auto Answer mode. When set to this mode, the data phone will automatically answer any incoming call when it detects a ringing signal on the line, provided that the AUTO button on the 201A data phone has also been left depressed.

DPØF 704702 Data Phone Off

Causes the Data Phone to hang up and ignore any new calls. Also prevents the Data Phone interface from issuing program interrupt requests.

DPRC 704714 Data Phone Read Character

The AC is cleared and one word which has been received by the interface is read into the AC. The bits 11-17 of the AC contain the character and bit 0 is 0 if the character was received with correct parity and 1 if the parity check failed. The Receiver flag goes down and stays down until another character has been received.

Not used DPMK 704744 Data Phone Mark

Causes the data phone to transmit a continuous stream of 1's.

not used DPQT 704721 Data Phone Quiet

Causes the DP to stop transmitting 1's and go to the receive state, if it is wired for half duplex operation

DPWC 704722 Data Phone Write Character

Bits 11-17 of the Ac are transfered to the interface where a parity bit is automatically added and the character is then transmitted. The transmitter flag goes down and stays down until the transmitter is ready for another character.

DPBS 704724 Data Phone Break Synchronization

Intended for use primarily in the full duplex mode. Is used to break the receiver synchronization. The receiver will then ignore all incoming data until it detects two adjacent Synch characters. (The Synch character is 026_8 or 0010110_2)

DPSF 704741 Data Phone Skip on Flag

If the Data Phone Flag is raised, the next instruction will be skipped. The Data Phone Flag will be raised if the DPØN instruction has been issued and one or more of the following have occurred:

(1) There has been an ON transition of the Receiver Flag

(2) There has been an ON transition of the Transmitter Flag

(3) The state of the Interlock has changed

(4) The state of the Carrier has changed

(5) The Data Phone is ringing

DPRS 704752 Data Phone Read Status

The AC is cleared and a Data Phone Status word is then read into it. The format of the status word is shown below

AC bit	0	1	2	3	4	5	6
SIGNAL	REC FLG	XMIT FLG	CAR-RIER	INTERLOCK	RING	SYNC	CLEAR TO SEND

DPCF 704761 Data Phone Clear Flag

The Data Phone Flag is cleared

TIMING CONSIDERATIONS

Since the Data Phone receives or transmits in a bit-synchronous mode, the computer must respond to the receiver and transmitter flags within 3.75 ms of the time they are raised or errors will be present in the received or transmitted data.

SYNCHRONIZING

To establish synchronization between the near and remote data phone terminals, each new message should be preceeded by a minimum of two sync characters (026). The receiver automatically removes the first two sync characters from the received message and does not pass them on to the computer.

CONTROL SIGNALS

Carrier

Will be present just before, during, and for a short while after a message is being transmitted or received.

Interlock

Will be present if the data phone thinks it has a good connection to another phone. The Interlock Signal will disappear if the connection is broken.

Ring

Appears if the Data Phone is ringing.

Sync

Tells if the receiver is synchronized to an incoming data stream.

Clear to Send

Says that the local data phone is in the transmitting state and ready to accept data from the interface. There will be a delay between the time the first DPWC instruction used to transmit a message is given and the time the Clear to Send signal comes ON.

PARITY

At present the data phone interface sends and receives using odd parity. It is possible that at a future date the following IOT instructions will be added to allow use of odd or even parity.

not used

DPEP 704762 Data Phone Even Parity

Send and receive all following messages using even parity.

DPØP 704764 Data Phone Odd Parity

Send and receive all following messages using odd parity.

This modification will be added if required at any time in the future. To insure that any programs written now will continue to work if the modification is installed, all current programs should include the DPØP instruction in the initialization block.

TRANSMITTING SEQUENCE

Messages are sent and received with the least significant bit first, followed by bits of increasing significance and finally the parity bit.

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BELL TELEPHONE LABORATORIES
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SUBJECT: GRAPHIC-2 IOT Instructions

DATE: September 25, 1967

FROM: W.H.Ninke
P.E.Rosenfeld

In the following discussion of the GRAPHIC-2 IOT instructions, the word "instruction" refers to a PDP-9 IOT, while the word "command" refers to a display command(executed from the display buffer). The IOT's are given below in ascending numerical order.

In assigning mnemonics to the IOT instructions, the following conventions have been observed. A transfer from the accumulator (AC) to another register is called writing, and all instructions which write start with W. A transfer into the accumulator from another register is called loading and instructions which load start with L. A single status bit which can be controlled by IOT's is turned on by an instruction starting with E for Enable and is turned off by an instruction starting with D for Disable. A flag is cleared by an instruction starting with C (except for CØN).

CDF	700501	Clear Display Flags. The light-pen, edges, stop, conditional-stop, immediate-stop, and display-trap flags are turned off. The vector-component holding registers are cleared. The display cycle control is set to single-step operation.
WDA	700502	Write Display Address. The 13 low-order bits of the AC are written into the display address register.

ECR	700504	Enable Continuous Run. The cycle control is set to the continuous-run state.
ESS	700524	Enable Single-Step. The cycle control is set to the single-step state.

To start the scope after a display-trap flag, stop flag or conditional-stop flag has stopped the cycling, the following instruction is used:

CØN	700545	CONtinue. A CDF is performed. The cycle control is set to the continuous-run state and the data-request signal is turned on. The display starts at the location currently in the display address register.

To start the scope at a specific address, the following instruction is used:

BEG	700547	BEGin. (WDA followed by CØN). The display is started at the location specified by the 13 low-order bits of the AC.
WDBC	700605	Write Display Buffer and Continue. The contents of the AC are written into the display buffer register. The data-request signal is turned off. The display cycle control is set to the continuous-run state. Execution of the command transferred to the display buffer is begun. When this command is completed, the next command will be

taken from the location indicated by the display address register and normal continuous cycling will then take place.

LDB	700612	Load Display Buffer. The display buffer register is loaded into the AC.
WDBS	700625	Write Display Buffer and Single-Step. The contents of the AC are written into the display buffer register. The data-request signal is turned off. The display cycle control is set to the single-step state. Execution of the command transferred to the display buffer is begun. When this command is completed, the data-request signal is turned on and the display awaits further instructions.
ELP	700701	Enable the Light Pen. The light pen is activated so that light sensed within the field of view of the pen will turn the light-pen flag on. This function can also be accomplished using a parameter-mode display command.
DLP	700721	Disable the Light Pen. The light pen is disabled so that light sensed within the field of view of the pen will not turn the light-pen flag on. This function can also

be performed by a parameter-mode display command.

Note: The ability of the pen to respond to light within the field of view is determined by the last LP control IOT or parameter-mode display command (with LP control bits set) that has been given. Thus, if a parameter-mode word enables the light pen and a DLP instruction is then executed by the computer, the pen is disabled until another parameter-mode word or IOT changes the status of the pen.

RLPE	700722	Resume after Light Pen stoppage with pen Enabled. The light-pen flag stops the display. This instruction causes resumption from the exact point of stoppage. The light-pen flag is turned off and the light pen is left enabled.
RLPD	700723	Resume after Light Pen stoppage with pen Disabled. Same as RLPE except the light pen is disabled.
RAEF	700742	Resume After Edges Flag. The edges flag stops the display. This instruction causes resumption from the exact point of stoppage. All edge flags are cleared.

Note: If an RLPD or RLPE is given with the edges flag on, the display will not resume until an RAEF is also given. Similarly, with the light-pen flag on, an RAEF will not cause resumption until an RLPE or RLPD is given. This

method of operation allows the light-pen-flag programming and the edge-flag programming to be separate uncoupled modules. Simultaneous light-pen flag and edges flag will not cause problems in the order of processing.

ECS 701001 Enable Conditional Stop. The conditional-stop feature for slave-mode words is enabled.

LDA 701012 Load Display Address. The display address register is loaded into the 13 low-order bits of the AC. The 5 high-order bits of the AC are cleared. The display address register always points one beyond the display command being executed under normal cycling.

DCS 701021 Disable Conditional Stop. The conditional-stop feature for slave-mode words is disabled.

LPM 701032 Load Parameter-Mode command. The parameters settable by a parameter-mode command are loaded into the AC in the following format: The prefix 0001 is loaded into the high-order bits. Bits 4,6,8,12 and 15 are set to 1. The remaining bits are loaded as follows:

AC5 - Blink
AC7 - LP enable
AC9 - Exchange axis
AC10 - Complement X component
AC11 - Complement Y component
AC13-- Scale 0
AC14 - Scale 1
AC16 - Intensity 0
AC17 - Intensity 1

Thus, the parameters are loaded in the format of a parameter-mode command.

LDS 701052 Load Display Status. The display flags and conditions are loaded into the AC in the following format:

	Bit is 0	Bit is 1
AC0 - Display-Trap Flag	off	on
AC1 - Edges Flag	off	on
AC2 - Light-Pen Flag	off	on
AC3 - Stop Flag	off	on
AC4 - Conditional-Stop Flag	off	on
AC5 - Pushbuttons Flag	off	on
AC6 - Console-Keyboard Flag	off	on
AC7 - Data-Phone Flag	off	on
AC8 - Byte Scan	1st byte	2nd byte
AC9 - Conditional-Stop Enable	off	on
AC10 - Immediate Stop	off	enabled
AC11 - Cycle Control	continuous	single-step
AC12 - Data Request	busy	ready
AC13 - Override	disabled	enabled
AC14 - Right Edge Flag	off	on
AC15 - Left Edge Flag	off	on
AC16 - Top Edge Flag	off	on
AC17 - Bottom Edge Flag	off	on

EIS 701401 Enable Immediate Stop. The immediate-stop condition is enabled. If this instruction is issued during the execution of a Load-X-or-Y-and-Wait command, the display should not be restarted for at least 35 usec (to allow completion of the Wait).

LX 701412 Load X. The X deflection register is loaded into the low-order 10 bits of the AC. The high-order 8 bits are cleared.

EØV 703401 Enable OVerride. The override condition is enabled (scope beam turned off).

LY 703412 Load Y. The Y deflection register is loaded into the low-order 10 bits of the AC. The high-order 8 bits are cleared.

DØV	703421	Disable OVerride. The override condition is disabled (scope beam turned on).
SCK	704301	Skip On Console-Keyboard flag. If the console-keyboard flag is on indicating that a key has been depressed, the next instruction is skipped.
ØCK	704302	Or Console Keyboard. The code for the currently depressed key is or-gated into the AC. If no key is currently depressed, the AC is unchanged. The bit format is as follows: AC11 - KB0 AC12 - KB1 AC13 - KB2 AC14 - KB3 AC15 - KB4 AC16 - KB5 AC17 - KB6
CCK	704304	Clear Console Keyboard. The console-keyboard flag is cleared.
LCK	704312	Load Console Keyboard. The AC is cleared and then an ØCK is performed.
SPB	704401	Skip on Push-Buttons flag. If the pushbuttons flag indicating that any pushbutton has been pushed is on, the next instruction is skipped.

ØPB	704402	Or Push Buttons. The status of the pushbuttons is or-gated into the AC. If no pushbutton is currently depressed, the AC is unchanged. The bit format is as follows: AC0 - PB0 AC1 - PB1 AC2 - PB2 AC3 - PB3 AC4 - PB4 L AC5 - PB5 R AC6 - PB6 AC7 - PB7
CPB	704404	Clear Push Buttons. The pushbuttons flag is cleared.
LPB	704412	Load Push Buttons. The AC is cleared and then an ØPB is performed.
WBL	704424	Write Button Lights. The lights in the pushbuttons corresponding to the 1-bits in the AC are turned on. The previous status of the lights is lost. The bit format for the lights is the same as for the corresponding pushbuttons as given in ØPB.
LBL	704432	Load Push Button Lights. The AC is cleared. The pushbutton lights status is loaded into the AC. The bit format is the same as for the corresponding pushbuttons as given in ØPB.

Note: The following IOT (7045xx) applies only to the PDP-7 implementation.

EIM 704501 — Enable the Interrupt Mask. Those bits in the interrupt mask corresponding to 1-bits in the AC are turned on. Any previously enabled interrupts remain enabled. The bit assignment from the AC is:

AC0 - Display-Trap Flag
AC1 - Edges Flag
AC2 - Light-Pen Flag
AC3 - Stop Flag
AC4 - Conditional-Stop Flag
AC5 - Pushbutton Flag
AC6 - Console-Keyboard Flag
AC7 - Data-Phone Flag

LIM 704512 — Load Interrupt Mask. The interrupt mask is loaded into the AC. The bit format is the same as for the control formats given for EIM. The remaining bits of the AC are cleared.

DIM 704521 — Disable Interrupt Mask. Those bits of the interrupt mask corresponding to 1-bits in the AC are turned off. Any previously disabled interrupts remain disabled. AC bit assignment is the same as for EIM.

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INPUT/OUTPUT TRANSFER INSTRUCTIONS (cont.)

Mnemonic	Code	Operation	Cycles
		CARD READERS	
CRSF	706701	Skip if card reader flag = 1.	1
CRSA	706704	Select and read alphanumeric.	1
CRRB	706712	Read the card reader buffer.	1
CRSB	706744	Select and read binary.	1
		DECtape SYSTEM	
MMRD	707512	Read one word into AC.	1
MMWR	707504	Write one word from AC.	1
MMSE	707644	Select transport from AC 2-5.	1
MMLC	707604	Set DECtape control from AC 12-17.	1
MMRS	707612	Read status bits into AC 0-5.	1
MMDF	707601	Skip on DECtape data flag.	1
MMBF	707601	Skip on DECtape block end flag.	1
MMEF	707541	Skip on DECtape error flag.	1

MODEL 33 ASR/KSR TELETYPE CODE (ASCII) IN OCTAL FORM

Character	8-Bit Code (in Octal)	Character	8-Bit Code (in Octal)
A	301	!	241
B	302	"	242
C	303	#	243
D	304	$	244
E	305	%	245
F	306	&	246
G	307	'	247
H	310	(	250
I	311	)	251
J	312	*	252
K	313	+	253
L	314	,	254
M	315	-	255
N	316	.	256
O	317	/	257
P	320	:	272
Q	321	;	273
R	322	<	274
S	323	=	275
T	324	>	276
U	325	?	277
V	326	@	300
W	327	[	333
X	330	\	334
Y	331	]	335
Z	332	↑	336
		←	337
0	260	Leader/Trailer	200
1	261	Line-Feed	212
2	262	Carriage-Return	215
3	263	Space	240
4	264	Rub-out	377
5	265	Blank	000
6	266	EOT	204
7	267	WRU	205
8	270	RU	206
9	271	Bell	207
		Act Mode	375

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PDP-7

INSTRUCTION LIST

MEMORY REFERENCE INSTRUCTIONS

Mnemonic	Code	Operation	Cycles*
CAL	00	Call subroutine	2
DAC	04	Deposit accumulator	2
JMS	10	Jump to subroutine	2
DZM	14	Deposit zero in memory	2
LAC	20	Load accumulator	2
XOR	24	Boolean exclusive OR	2
ADD	30	Add, 1's complement	2
TAD	34	Add, 2's complement	2
XCT	40	Execute	1**
ISZ	44	Increment and skip if zero	2
AND	50	Boolean AND	2
SAD	54	Skip if AC different from memory	2
JMP	60	Jump	1

* Cycle time is 1.75 microseconds.

** Plus execution time of instruction referenced.

Indirect addressing: Adding "I" to any memory reference instruction, e.g., DZM I Y, causes C(Y) to be taken as the effective address, and adds 1 cycle to the execution time.

OPERATE INSTRUCTIONS

Mnemonic	Code	Operation Executed	Event Time
OPR or NOP	740000	Operate group or no operation.	—
CMA	740001	Complement accumulator.	3
CML	740002	Complement link.	3
OAS	740004	Inclusive OR AC switches with AC.	3
RAL	740010	Rotate AC and link left.	3
RAR	740020	Rotate AC and link right.	3
HLT	740040	Halt.	1
SMA	740100	Skip if AC<0.	1
SZA	740200	Skip if AC=0.	1
SNL	740400	Skip if link≠0.	1
SKP	741000	Skip unconditionally.	1
SPA	741100	Skip if AC positive.	1
SNA	741200	Skip if AC≠0.	1
SZL	741400	Skip if link=0.	1
RTL	742010	Rotate AC and L left two places.	2,3
RTR	742020	Rotate AC and L right two places.	2,3
CLL	744000	Clear link.	2
STL	744002	Set link=1.	2,3
RCL	744010	Clear link, then rotate AC and L left.	2,3
RCR	744020	Clear link, then rotate AC and L right.	2,3
CLA	750000	Clear AC.	2
CLC	750001	Clear and complement AC.	2,3
LAS	750004	Load AC from switches.	2,3
GLK	750010	Get link into AC 17.	2,3
LAW	76XXXX	Load the AC with LAW XXXX.	—

EAE INSTRUCTIONS

Mnemonic	Code	Operation	Time (usec)
EAE	640000	No operation.	1.75
LRS	640500	Long right shift.	1.6+0.1n
LRSS	660500	Long right shift, signed.	1.6+0.1n
LLS	640600	Long left shift.	1.6+0.1n
LLSS	660600	Long left shift, signed.	1.6+0.1n
ALS	640700	Accumulator left shift.	1.6+0.1n
ALSS	660700	Accumulator left shift, signed.	1.6+0.1n
NORM	640444	Normalize, unsigned.	1.6+0.1n
NORMS	660444	Normalize, signed.	1.6+0.1n
MUL	653122	Multiply, unsigned.	1.6+0.1n
MULS	657122	Multiply, signed.	2.4+0.1n+0.25m
DIV	640323	Divide, unsigned.	2.4+0.1n+0.25m
DIVS	644323	Divide, signed.	2.4+0.35n+0.2m
IDIV	653323	Integer divide, unsigned.	2.4+0.35n+0.2m
IDIVS	657323	Integer divide, signed.	2.4+0.35n+0.2m
FRDIV	650323	Fraction divide, unsigned.	2.4+0.35n+0.2m
FRDIVS	654323	Fraction divide, signed.	2.4+0.35n+0.2m
LACQ	641002	Load AC with C(MQ).	1.75
LACS	641001	Load AC with C(SC).	1.75
CLQ	650000	Clear MQ.	1.75
ABS	644000	Take absolute value of AC.	1.75
GSM	664000	Get sign and magnitude.	1.75
OSC	640001	Inclusive OR the SC into the AC.	1.75
OMQ	640002	Inclusive OR the MQ into the AC.	1.75
CMQ	640004	Complement the MQ.	1.75
LMQ	652000	Load MQ with C(AC).	1.75

n=shift count
m=one bits in multiplier quotient

INPUT/OUTPUT TRANSFER INSTRUCTIONS

Mnemonic	Code	Operation	Cycles
		PROGRAM INTERRUPT	
IOF	700002	Interrupt off. Disable the PIC.	1
ION	700042	Interrupt on. Enable the PIC.	1
ITON	700062	Interrupt and trap on.	1
		REAL TIME CLOCK	
CLSF	700001	Skip if clock flag=1.	1
CLOF	700004	Clear flag and disable the clock.	1
CLON	700044	Clear flag and enable the clock.	1
		PERFORATED TAPE READER	
RSF	700101	Skip if reader flag=1.	1
RCF	700102	Inclusive OR reader buffer into AC and clear flag.	1
RRB	700112	Read reader buffer and clear reader flag.	1
RSA	700104	Reader in alphanumeric.	1
RSB	700144	Reader in binary.	1

INPUT/OUTPUT TRANSFER INSTRUCTIONS (cont.)

Mnemonic	Code	Operation	Cycles
		PERFORATED TAPE PUNCH	
PSF	700201	Skip if punch flag=1.	1
PCF	700202	Clear punch flag.	1
PSA or PLS	700204	Punch alphanumeric.	1
PSB	700244	Punch binary.	1
		I/O EQUIPMENT	
IORS	700314	Input/output read status.	1
TTS	703301	Skip if KSR 33 is used.	1
CAF	703302	Clear all flags.	1
SKP7	703341	Skip if processor is a PDP-7.	1
		TELETYPE KEYBOARD	
KSF	700301	Skip if keyboard flag=1.	1
KRB	700312	Read the keyboard buffer and clear flag.	1
		TELETYPE TELEPRINTER	
TSF	700401	Skip if teleprinter flag=1.	1
TCF	700402	Clear the teleprinter flag.	1
TLS	700406	Load teleprinter buffer, select and print.	1
		OSCILLOSCOPE DISPLAY TYPE 34A AND PRECISION CRT DISPLAY TYPE 30D	
DXC	700502	Clear X-coordinate buffer.	1
DYC	700602	Clear Y-coordinate buffer.	1
DXL	700506	Load X-coordinate buffer.	1
DYL	700606	Load Y-coordinate buffer.	1
DXS	700546	Load X-coordinate buffer and display.	1
DYS	700646	Load Y-coordinate buffer and display.	1
DSF	700701	Skip if display flag=1.	1
DCF	700702	Clear display flag.	1
DLB	700706	Load brightness register.	1
ADRM	701214	Read MX address.	1
		GENERAL PURPOSE MULTIPLEXER CONTROL TYPE 139	
ADSM	701103	Select MX channel.	1
ADIM	701201	Increment channel address.	1
		ANALOG-TO-DIGITAL CONVERTERS	
ADSF	701301	Skip if converter flag=1.	1
ADSC	701304	Select and convert.	1
ADRB	701312	Read converter buffer.	1
		AUTOMATIC PRIORITY INTERRUPT TYPE 172	
CAC	705501	Clear all channels.	1
ASC	705502	Enable selected channel(s).	1
DSC	705604	Disable selected channel(s).	1
EPI	700044	Enable API.	1
DPI	700004	Disable API.	1
ISC	705504	Initiate break on selected channel.	1
DBR	705601	Debreak.	1
		MEMORY EXTENSION CONTROL TYPE 146	
SEM	707701	Skip if in extend mode.	1
EEM	707702	Enter extend mode.	1
LEM	707704	Leave extend mode.	1
EMIR	707742	Extend mode interrupt restore.	1