Sound Blaster Pro Master Volume Emulation

Sound Blaster Pro emulations for master volume means that the 6-bit volume counters can be written via the Sound Blaster Pro Mixer register 22h (or 32h). Sound Blaster Pro emulation is enabled by default, and can be disabled by setting bit 0 of Mixer register 64h.

The master volume registers 60h and 62h can always be read, regardless of whether Sound Blaster Pro volume emulation is enabled, using the Sound Blaster Pro Mixer registers 22h (and 32h). The following 6-bit to 4-bit translation table is used:

Table 1 SB Pro Master Read Volume Emulation

Mute	Master Volume	Value Read at 32h	Value Read at 22h
1	xx	0	1
0	0-24	1	1
0	25-30	2	3
0	31-34	3	3
0	35-38	4	5
0	39-42	5	5
0	43-46	6	7
0	47-50	7	7
0	51-54	8	9
0	55	9	9
0	56-57	10	11
0	58	11	11
0	59-60	12	13
0	61	13	13
0	62	14	15
0	63	15	15

If Sound Blaster Pro volume emulation is enabled, then a mixer reset will cause both left and right channels to set to their power-on defaults, namely 54 (36h).

If Sound Blaster Pro volume emulation is enabled, then a write to mixer register 22h (or 32h) will cause both the left and right master volume registers to be changed as follows:

Table 2 SB Pro Write Volume Emulation

Value written to 22h or 32h	Mute	6-bit Volume
0	1	24
1	0	24
2	0	30
3	0	34
4	0	38
5	0	42
6	0	46
7	0	50
8	0	54
9	0	55
10	0	56
11	0	58
12	0	59
13	0	61
14	0	62
15	0	63

REGISTERS

Types of Register Access

There are two types of audio registers in the ES1887:

- Mixer registers.

  These registers are accessed via I/O ports Audio_Base+4h and Audio_Base+5h. Audio_base+4h is written with the register address. Then the register can be read/written via Audio_Base+5h. These registers control many functions other than the mixer.

- Controller registers

  These registers are used to control Extended mode DMA playback and record through the first audio channel. Controller registers are accessed via an extension to the Sound Blaster common interface. This interface uses I/O ports Audio_Base+Ah, Audio_Base+Ch, and Audio_Base+Eh to transfer read data, write data/commands, and status respectively.

Mixer Registers

There are two types of mixer registers. Sound Blaster Pro Compatible mixer registers, as the name suggests are fully compatible with the Sound Blaster Pro. ESS mixer registers are specific to ESS Technology, Inc. ES1887 *Audio***Drive**® chips; though many registers are shared throughout the *Audio***Drive**® family of chips.

Sound Blaster Pro Compatible Mixer Registers

This section provides a summary of Sound Blaster Pro compatible mixer registers in the ES1887 and some comments on the characteristics of these registers.

Table 3 Sound Blaster Pro Compatible Register Summary

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Remark
00h	Write: reset mixer								Mixer reset
04h	DAC play volume left			x	DAC play volume right			x	DAC playback volume
0Ah	x	x	x	x	x	Mic mix volume		x	Mic mix volume
0Ch	x	x	F1[a]	x	F0[a]	ADC Source		x	See note for F0, F1.
0Eh	x	x	F2[a]	x	x	x	Stereo	x	See note for F2.
22h	Master volume left			x	Master volume right			x	Master volume
26h	FM volume left			x	FM volume right			x	Music DAC volume
28h	CD (AuxA) volume left			x	CD (AuxA) volume right			x	CD (AuxA) Volume
2Eh	Line volume left			x	Line volume right			x	Line volume

a. Sound Blaster filter control bits F2, F1, and F0 have no function in the ES1887 and are ignored.

Filter Control Bits

The Sound Blaster Pro mixer has three bits that control input and output filters. They are labeled as F0, F1, and F2 in Table 3 and Table 4. They have no function in the ES1887 and their values are ignored.

Mixer Stereo Control Bit

Bit 1 of register 0Eh is the Mixer Stereo Control bit. It is normally zero. Set this bit high to enable Sound Blaster Pro compatible stereo DAC functions. Program the DAC sample rate to be twice the sample rate of each channel. For example, for 22 kHz stereo, program the “sample rate” to be 44 kHz using command 40h.

This bit enables stereo only for DMA transfer to the DAC in Compatibility mode. It should not be used in Extended mode.

Clear this bit after completing the stereo DMA transfer, because this bit is unaffected by software reset (only mixer reset).

See also “Stereo DMA Transfers in Compatibility Mode” on page 29.

ESS Mixer Registers

This section provides a summary of the ESS mixer registers followed by a detailed description of each register.

Table 4 ESS Mixer Register Summary

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Remark
00h	Write: reset mixer								Reset mixer
14h	Audio 1 play volume left				Audio 1 play volume right				Audio 1 play volume
1Ah	Mic mix volume left				Mic mix volume right				Mic mix volume
1Ch	x	x	F1[a]	x	F0[a]	Record source			Record source select
1Eh	x	x	F2[a]	x	x	x	Stereo	x	Stereo flag
32h	Master volume left				Master volume right				Master volume
36h	FM volume left				FM volume right				FM volume
38h	CD (AuxA) volume left				CD (AuxA) volume right				CD volume
3Ah	AuxB volume left				AuxB volume right				AuxB volume
3Ch						PC speaker volume			PC speaker volume
3Eh	Line volume left				Line volume right				Line volume
40h	MPU-401 enable and IRQ select			MPU-401 address		Restart configuration	Joystick enable	FM enable	FM/Joystick/MPU-401 configuration
42h	Input override	Preamp bypass	Input source		Input volume				Serial mode input control
44h	Output override	Output signal			Output volume				Serial mode output control
46h	Analog control override	0	Left ADC	Right ADC	Analog control		FDXO enable	FDXI enable	Serial mode miscellaneous analog control
48h	SE enable	Data format	Serial reset	ES689/ ES69x interface enable	Active low sync	DSP test mode	Telegaming mode enable	0	Serial mode miscellaneous control
4Ch	Filter override	0			2's complement filter divider				Serial mode filter divider control
4Eh	Transmit source		Transmit length	Transmit mode	Receive source		Receive length	Receive mode	Serial mode format/source/target control
60h	0	Mute	Left master volume						Left master volume counter value
62h	0	Mute	Right master volume						Right master volume counter value
64h	HWV operation mode		Volume count	HWV IRQ flag	0	Enable HWV IRQE	HWV interrupt mask	SB Pro master volume disable	Master volume control
66h	Write: Reset hardware volume interrupt request								Hardware volume interrupt request
68h	Mic mix volume left				Mic mix volume right				Mic record volume
69h	Audio 2 volume left				Audio 2 volume right				Audio 2 record volume
6Ah	CD (AuxA) volume left				CD (AuxA) volume right				CD (AuxA) record volume
6Bh	FM volume left				FM volume right				Music DAC record volume
6Ch	AuxB volume left				AuxB volume right				Aux B record volume
6Eh	Line volume left				Line volume right				Line record volume
70h	Clock source	Sample rate divider							Audio 2 sample rate divider
72h	Filter clock divider								Audio 2 filter clock divider
74h	2's complement transfer count – low byte								Audio 2 transfer count reload
76h	2's complement transfer count – high byte								

Table 4 ESS Mixer Register Summary (Continued)

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Remark
78h	DMA transfer type		DMA transfer length	Auto-initialize enable	Resume flag	Suspend flag	Enable transfer into FIFO	Enable transfer to DAC	Audio 2 control 1
7Ah	IRQ latch	IRQE enable	DRQ/ DACKB enable	Mixer source		FIFO signed mode	FIFO stereo mode	FIFO 16-bit mode	Audio 2 control 2
7C	Audio 2 volume left				Audio 2 volume right				Audio 2 playback volume
7Dh	0				FM mix enable	DRQ pull-down enable	DRQ/DACKB select		Audio 2 Configuration
7Fh	MPU-401 IRQ	HWV IRQ	Audio 2 IRQ	Audio 1 IRQ	Interrupt select			Output enable	Interrupt Control

a. Sound Blaster filter control bits F2, F1, and F0 have no function in the ES1887 and are ignored.

Register Detailed Descriptions

Reset Mixer (00h, R/W)

Write: Reset Mixer							
7	6	5	4	3	2	1	0

Audio 1 Playback Volume (14h, R/W)

Audio 1 play volume left				Audio 1 play volume right			
7	6	5	4	3	2	1	0

This register controls the playback volume of the first audio channel. On reset, this register assumes the value of 88h.

Mic Mix Volume (1Ah, R/W)

Mic mix volume left				Mic mix volume right			
7	6	5	4	3	2	1	0

This register controls the playback volume of the Mic input. On reset, this register assumes the value of 00h.

Record Source Select (1Ch, W)

x	x	F1	x	F0	Record Source		
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 00h.

Bits Definitions:

Bits	Name	Description
7:6	–	No function.
5	F1	Sound Blaster Pro filter control bit. Has no function in the ES1887 and is ignored.
4	–	No function.
3	F0	Sound Blaster Pro filter control bit. Has no function in the ES1887 and is ignored.
2:0	Record Source	For extended access, use register address 1Ch to select recording from the mixer as follows:

bit 2	bit 1	bit 0	record source selected
x	0	x	Microphone (default)
0	1	x	CD (AuxA) input
1	1	0	Line input
1	1	1	Mixer

Bits 4:3 of Register 7Ah determines if mixer input source is Record or Playback Mixer.

Stereo Flag (1Eh, R/W)

x	x	F2	x	x	x	Stereo flag	x
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 00h.

Bits Definitions:

Bits	Name	Description
7:6	–	No function.
5	F2	Sound Blaster Pro filter control bit. Has no function in the ES1887 and is ignored.
4:2	–	No function.
1	Stereo Flag	1 = Enable Sound Blaster Pro compatible stereo DAC functions. 0 = Disable Sound Blaster Pro compatible stereo DAC functions.
0	–	No function.

Master Volume (32h, R/W)

Master volume left				Master volume right			
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 88h.

This register provides backward compatible access to master volume. New applications can also use registers 60h and 62h which have more resolution.

FM Volume (36h, R/W)

FM volume left				FM volume right			
7	6	5	4	3	2	1	0

This register controls the playback volume of the music DAC. On reset, this register assumes the value of 88h.

CD (AuxA) Volume (38h, R/W)

CD (AuxA) volume left				CD (AuxA) volume right			
7	6	5	4	3	2	1	0

This register controls the playback volume of the CD audio input. On reset, this register assumes the value of 00h.

AuxB Volume (3Ah, R/W)

AuxB volume left				AuxB volume right			
7	6	5	4	3	2	1	0

This register controls the playback volume of the auxiliary line input. On reset, this register assumes the value of 00h.

PC Speaker Volume (3Ch, R/W)

					PC speaker volume		
7	6	5	4	3	2	1	0

This register controls the PC speaker volume. Bits 2:0 select the attenuation level in steps of -3 dB. The maximum setting of 08h corresponds to 0 dB attenuation. On reset, this register assumes the value of 04h.

Line Volume (3Eh, R/W)

Line volume left				Line volume right			
7	6	5	4	3	2	1	0

This registers controls the playback volume of the line input. On reset, this register assumes the value of 00h.

FM/Joystick/MPU-401 Configuration (40h, R/W)

MPU-401 enable and IRQ select			MPU-401 address		Restart configu-ration	Joystick enable	FM enable
7	6	5	4	3	2	1	0

Bits 7:3 and Bits 1:0 are cleared by hardware reset. This register is not affected by a mixer reset command (register 00h).

Bits Definitions:

Bits	Name	Description
7:5	MPU-401 enable and IRQ select	Enables MPU-401 and select interrupt channel: bit 7 / bit 6 / bit 5 / function 0 0 0 MPU-401 disabled* 0 0 1 MPU-401 enabled/No IRQ 0 1 0 Share IRQ with audio 0 1 1 IRQE 1 0 0 IRQA 1 0 1 IRQB 1 1 0 IRQC 1 1 1 IRQD *Disabled is MPU-401 hardware reset default.
4:3	MPU-401 address	Selects MPU-401base address: bit 4 / bit 3 / address 0 0 300h 0 1 310h 1 0 320h 1 1 330h
2	Restart configu-ration	(Write Only) Used for the ES1888 Compatible Read-Sequence-Key method of software address selection. In this case, writing this bit high puts the ES1887 in its disabled state in anticipation of a new read-sequence-key. The read-sequence-key is used to change the base register address. See “ES1888 Compatible Read-Sequence-Key Method” on page 22.
1	Joystick enable	(R/W) For backward compatibility to the ES1888, this bit, when high, enables the decode of register address 201h for read and write to access the internal joystick port. Setting this bit high overrides enable or address selected via SCR 0 bits 5:3 of 0E1h.
0	FM enable	(R/W) For backward compatibility to the ES1888, this bit, when high enables the decode of register addresses 388h-3B8h for the internal FM synthesizer. It does not affect FM synthesizer addresses. These are offsets of the base register address. Setting this bit high enables FM alias at the base address specified by SCR 0 bits 7:6 of 0E1h.

Serial Interface Registers

This section describes registers related to the DSP and ES689/ES69x serial interface.

Serial Mode Input Control (42h, R/W)

Input override	Preamp bypass	Input source		Input volume			
7	6	5	4	3	2	1	0

Bits Definitions:

Bits	Name	Description
7	Input override	1 = Input source and input volume replace normal values as programmed by the application when the ES1887 is in serial mode. 0 = Input source and input volume are unchanged during serial mode.
6	Preamp bypass	1 = the 26 dB microphone preamp (if bit 7 is high) is bypassed during serial mode.
5:4	Input source	Input source selects the input source during serial mode if bit 7 is high. The values below override the normal mixer settings (register 0Ch or 1Ch): bit 5 / bit 4 / input source 0 0 Line 0 1 CD (AuxA) 1 0 Microphone 1 1 Mixer Bits 4:3 of Register 7Ah determines if the mixer input source is Record or Playback Mixer.
3:0	Input volume	If bit 7 is high during serial mode, this value overrides the input volume settings set via controller register B4h.

Serial Mode Output Control (44h, R/W)

Output override	Output signal			Output volume			
7	6	5	4	3	2	1	0

Bits Definitions:

Bits	Name	Description
7	Output override	1 = Output volume during serial mode is from this register rather than from the Mixer Master Volume register. Output signal control is always in force during serial mode regardless of the state of this bit. 0 = Output volume is unchanged during serial mode.
6:4	Output signal	Controls the signal routed to speaker outputs AOUT_L and AOUT_R: bit 6 bit 5 bit 4 signal 0 0 0 Mute 0 0 1 Reserved. 0 1 0 Audio 1 DAC right channel played mono left and right. 0 1 1 Reserved. 1 0 0 Playback mixer output 1 0 1 Playback mixer output except Audio 1 DAC playback. 1 1 0 Reserved. 1 1 1 Reserved.
3:0	Output volume	Replaces normal master volume setting if bit 7 is high during serial mode.

Serial Mode Miscellaneous Analog Control (46h, R/W)

Analog control override	0	Left ADC	Right ADC	Analog control		FDXO enable	FDXI enable
7	6	5	4	3	2	1	0

Bits Definitions:

Bits	Name	Description
7	Analog override	1 = Bits 6:0 take effect during serial mode. 0 = Bits 6:0 do not take effect during serial mode.
6	–	Reserved. Always write 0.
5	Left ADC	1 = Left channel combined ADC and DAC is in ADC mode. 0 = Left channel combined ADC and DAC is in DAC mode.
4	Right ADC	1 = Right channel combined ADC and DAC is in ADC mode. 0 = Right channel combined ADC and DAC is in DAC mode.
3:2	Analog control	These special control signals control interconnections in the analog circuitry. They should be set appropriately for the application as follows: bit 3 bit 2 application 0 0 Stereo wave playback or record. 0 1 Reserved. 1 0 Full-duplex (mono record and mono playback). 1 1 Mono wave playback or record.
1	FDXO enable	1 = Enables FDXO output connection to output pin FOUT_R (right channel filter output). 0 = FDXO has 50K pull-up to CMR.
0	FDXI enable	1 = Enables FDXI input connection from left channel filter input and thus to the input of the left channel ADC. 0 = FDXI input has 50K pull-up to CMR. The left channel filter input and ADC comes from the input volume stage as usual.

Serial Mode Miscellaneous Control (48h, R/W)

SE enable	Data format	Serial reset	ES689/ ES69x interface enable	Active low sync	DSP test mode	Telegaming mode enable	0
7	6	5	4	3	2	1	0

Bits Definitions:

Bits	Name	Description
7	SE enable	1 = Enable DSP serial port. This signal is synchronized with DCLK input rising edge. If DCLK is not running, enabling SE has no effect. 0 = Disable DSP serial port.
6	Data format	1 = Data format is 2's complement (signed). 0 = Data format is unsigned (offset binary).
5	Serial reset	1 = Reset Serial register left/right toggle flags. 0 = Release reset. Serial reset also inhibits FDXO connection to FOUT_R and “zeros” all shift registers.
4	ES689/ ES69x interface enable	1 = Enable ES689/ES69x serial interface. 0 = Disable ES689/ES69x serial interface.
3	Active low sync	1 = Active-low frame sync pulse. 0 = Active-high frame sync pulse.
2	DSP test mode	1 = Test mode: FSX, FSR, DCLK become outputs. 0 = Disable DSP test mode.
1	Telegaming mode enable	1 = Enables telegaming mode. In serial mode, connect first channel DMA (otherwise known as game-compatible DMA) to the system DAC. This allows game-compatible audio to be heard when in serial mode. The system DAC gets its filter clock and volume control from the first channel. 0 = In serial mode, the first channel DMA is not played. The second channel is connected to the system DAC.
0	–	Reserved. Always write 0.

Serial Mode Filter Divider (4Ch, R/W)

Filter override	0			2’s complement filter divider			
7	6	5	4	3	2	1	0

This register controls the filter clock rate during serial mode.

Bits Definitions:

Bits	Name	Description
7	Filter override	1 = During serial mode, the filter clock is generated by dividing down the serial clock. 0 = During serial mode, the filter clock is generated as follows: Generally, the filter roll-off should be positioned at 80% – 90% of the Sample_Rate/2 frequency. The ratio of the roll-off frequency to the filter clock frequency is 1:82. In other words, first determine the desired roll-off frequency by taking 80% of the Sample_Rate divided by 2, then multiply by 82 to find the desired Filter Clock frequency. Use the formula below to determine the closest divider: Filter_Clock_Frequency = 7.16 MHz / (256-Filter_Divider_Register)
6:4	–	Reserved. Always write 0.
3:0	2’s complement filter divider	These bits are a 2's complement (signed) value that divides the serial clock. The ratio of the filter -3 dB frequency to the filter clock is about 1:41. Examples: 02h (-14) External Serial Clock 2.048 MHz / 14 / 41 = 3568 Hz for 8000 Hz sample rate. 0Eh (-2) Internal Serial Clock 1.591 MHz / 2 / 41 = 19.4 kHz for 44,100 Hz sample rate. Note that the sample rate divider is an integer multiple of the filter divider for 44,100, which gives maximum performance of DACs and ADCs.

Serial Mode Format/Source/Target (4Eh, R/W)

Transmit source		Transmit length	Transmit mode	Receive source		Receive length	Receive mode
7	6	5	4	3	2	1	0

Bits Definitions:

Bits	Name	Description
7:6	Transmit source	Transmit register source: bit 7 bit 6 source 0 0 None: Transmit register held at "zero code. 0 1 FIFO. 1 0 Left ADC or stereo ADC transmission. 1 1 Right ADC.
5	Transmit length	1 = Transmit length is 16 bits, unsigned. 0 = Transmit length is 8 bits, unsigned.
4	Transmit mode	1 = Transmit mode is stereo. Left and right channels alternate, with left channel data preceding right channel data. 0 = Transmit mode is mono.
3:2	Receive target	Receive register target: bit 7 bit 6 target 0 0 None: Transmit register held at "zero code. 0 1 FIFO. 1 0 DAC (if mono, right channel receives data, left channel receives complement of data). 1 1 Music DAC (if mono, right channel receives data, left channel receives complement of data).
1	Receive length	1 = Receive length is 16 bits, unsigned. 0 = Receive length is 8 bits, unsigned.
0	Receive mode	1 = Receive mode is stereo. Left and right channels alternate, with left channel data preceding right channel data. 0 = Receive mode is mono.

Extended Mode Master Volume Control Registers

This section describes registers related to the Master Volume control in Extended mode. These registers are accessed via I/O addresses Audio_Base+4h and Audio_Base+5h.

Left Master Volume and Mute (60h, R/W)

0	Mute	Left master volume					
7	6	5	4	3	2	1	0

This register determines the master volume level for the left channel.

When in Sound Blaster Pro Compatibility mode, writes to registers 22h or 32h are translated into writes to 60h and 62h. See "Sound Blaster Pro Master Volume Emulation" on page 1. Writes to this register when in Compatibility made run the risk of being overwritten.

On hardware reset this register is set to 36h.

Bits Definitions:

Bits	Name	Description
7	–	Reserved. Always write 0.
6	Mute	1 = Enable left channel mute. 0 = Disable left channel mute.
5:0	Left master volume	Bits 5:0 select the attenuation level in steps of -1.5 dB. The maximum setting of 3Fh corresponds to 0 dB attenuation.

Right Master Volume and Mute (62h, R/W)

0	Mute	Right master volume					
7	6	5	4	3	2	1	0

This register determines the master volume level for the right channel.

When in Sound Blaster Pro Compatibility mode, writes to registers 22h or 32h are translated into writes to 60h and 62h. See "Sound Blaster Pro Master Volume Emulation" on page 1. Writes to this register when in Compatibility made run the risk of being overwritten.

On hardware reset this register is set to 36h.

Bits Definitions:

Bits	Name	Description
7	–	Reserved. Always write 0.
6	Mute	1 = Enable right channel mute. 0 = Disable right channel mute.
5:0	Right master volume	Bits 5:0 select the attenuation level in steps of -1.5 dB. The maximum setting of 3Fh corresponds to 0 dB attenuation.

Master Volume Control (64h, R/W)

HWV operation mode		Volume count	HWV IRQ flag	0	Enable HWV IRQE	HWV interrupt mask	SB Pro master volume disable
7	6	5	4	3	2	1	0

Bits Definitions:

Bits	Name	Description
7:6	HWV operation mode	Selects hardware volume operation mode: bit 7 / bit 6 / mode 0 0 Normal 3-wire mode (hardware reset default). 0 1 2-wire mode: UP and DOWN inputs low together act as a MUTE input low. 1 0 2-wire enabled, debounce disabled, auto-increment/decrement disabled. 1 1 Hardware volume control disabled.
5	Volume count	1 = Count up and down by 3 for each push of UP or DOWN buttons. 0 = Count up and down by 1 for each push of UP or DOWN buttons.
4	HWV IRQ flag	Read-only interrupt request from hardware volume event.
3	–	Reserved. Always write 0.
2	Enable HWV IRQE	When high, enables IRQE as an output for the hardware volume control interrupt. This bit is cleared by hardware reset.
1	HWV interrupt mask	When high, enables the hardware volume control to be shared with the audio interrupt. This bit is cleared by hardware reset.
0	SB Pro master volume disable	When low, a write to the SB Pro Master Volume register will be translated into a write to the hardware master volume counters, Mixer registers 60h and 62h. If high, the SB Pro Master Volume registers are, in effect, read-only. This bit is cleared by hardware reset.

Hardware Volume Interrupt Request Reset (66h, W)

Write: Reset hardware volume interrupt request							
7	6	5	4	3	2	1	0

Any write to this register resets the hardware volume interrupt request. This register is write-only.

Mic Record Volume (68h, R/W)

Mic record volume left				Mic record volume right			
7	6	5	4	3	2	1	0

This registers controls the record volume for the Mic input. Set low by hardware reset, but not by mixer reset.

Audio 2 Record Volume (69h, R/W)

Audio 2 record volume left				Audio 2 record volume right			
7	6	5	4	3	2	1	0

This register controls the record volume for the second audio channel. Set low by hardware reset, but not by mixer reset.

CD (AuxA) Record Volume (6Ah, R/W)

CD record volume left				CD record volume right			
7	6	5	4	3	2	1	0

This register controls the record volume for the CD input. Set low by hardware reset, but not by mixer reset.

Music DAC Record Volume (6Bh, R/W)

FM record volume left				FM record volume right			
7	6	5	4	3	2	1	0

This register controls the record volume for the music DAC (FM). Set low by hardware reset, but not by mixer reset.

AuxB Record Volume (6Ch, R/W)

AuxB record volume left				AuxB record volume right			
7	6	5	4	3	2	1	0

This register controls the record volume for the auxiliary line input. Set low by hardware reset, but not by mixer reset.

Line Record Volume (6Eh, R/W)

Line record volume left				Line record volume right			
7	6	5	4	3	2	1	0

This register controls the record volume for the line input. Set low by hardware reset, but not by mixer reset.

Audio 2 Mixer Registers

This section describes registers related to the second audio channel. These registers are accessed via I/O addresses Audio_Base+4h and Audio_Base+5h.

Audio 2 Sample Rate Generator (70h, R/W)

Clock source	Sample rate divider						
7	6	5	4	3	2	1	0

This register should be programmed for the sample rate for all DAC operations in extended mode.

The sample rate is determined by the two's complement divider in bits 7:0.

Sample_Rate = 397.7 kHz / (128-x) if bit 7 = 0.
= 795.5 kHz / (256-x) if bit 7 = 1.

where: x = value in bits 6:0 of register 70h.

Bits Definitions:

Bits	Name	Description
7	Clock source	1 = Clock source is 795.5 kHz for sample rates higher than 22 kHz. 0 = Clock source is 397.7 kHz. for sample rates lower than or equal to 22 kHz.
6:0	Sample rate divider	Signed sample rate divider.

Audio 2 Filter Clock Divider (72h, R/W)

Filter clock divider							
7	6	5	4	3	2	1	0

This register controls the low-pass frequency of the switch-capacitor filters inside the ES1887. Generally, the filter roll-off should be positioned at 80% – 90% of the Sample_Rate/2 frequency. The ratio of the roll-off frequency to the filter clock frequency is 1:82. In other words, first determine the desired roll-off frequency by taking 80% of the Sample_Rate divided by 2, then multiply by 82 to find the desired Filter Clock frequency. Use the formula below to determine the closest divider:

Filter_Clock_Frequency = 7.16 MHz / (256-Filter_Divider_Register)

Audio 2 Transfer Count Reload (74h, R/W)

2's complement transfer count – low byte							
7	6	5	4	3	2	1	0

NOTE: When suspend/resume bit is set, reading this register returns the current counter contents.

Audio 2 Transfer Count Reload (76h, R/W)

2's complement transfer count – high byte							
7	6	5	4	3	2	1	0

NOTE: When suspend/resume bit is set, reading this register returns the current counter contents.

Audio 2 Control 1 (78h, R/W)

DMA transfer type	DMA transfer length	Auto-initialize enable	Resume flag	Suspend flag	Enable transfer into FIFO	Enable transfer to DAC
7 6	5	4	3	2	1	0

This register is reset to all zero by hardware or software reset via bit 0 of port Audio_Base+6h.

Bits Definitions:

Bits	Name	Description
7:6	DMA transfer type	Selects single or demand transfer for the second audio channel: bit 7 / bit 6 / transfer type / bytes/DMA request 0 0 single 1 0 1 demand 2 1 0 demand 4 1 1 demand 8
5	DMA transfer length	1 = 16-bit DMA transfer. 0 = 8-bit DMA transfer.
4	Auto-initialize enable	1 = Auto-initialize mode. After the transfer counter rolls over to 0, it is automatically reloaded and DMA continues. The second channel interrupt flag is set high. 0 = Normal mode. After the transfer counter rolls over to 0, it is reloaded but DMA stops. Bit 1 of this register is cleared. The second channel interrupt flag is set high.
3	Resume flag	(Read Only) If bit 2 is set high, this flag goes low when a suspend request has completed. If bit 2 is low, this flag goes low when the FIFO is empty.
2	Suspend flag	1 = suspend alternate DMA request/hold DMA. If DMA is in progress, it halts at the nearest 4-byte boundary and bit 3 is cleared. If DMA is not in progress when this bit is set high (i.e. bit 1 is low), then setting this bit high keeps DMA requests from beginning when bit 1 is also set high, until bit 2 is cleared. This used for resume after suspend: 1. Bit 1 is cleared. 2. Bit 2 is set. 3. 74h/76h are set to count-in-progress. 4. Bit 1 is set, thereby latching count-in-progress into counter. 5. 74h/76h are set to reload value. 6. Bit 2 is cleared, allowing DMA to continue.
1	Enable transfer into FIFO	1 = Enable DMA transfer into FIFO. 0 = Disable DMA transfer into FIFO. This causes the DMA counter to be reloaded from the reload register. This bit is cleared automatically at the completion of a non-auto-init transfer.
0	Enable transfer to DAC	1 = Enable transfer from FIFO to DAC. 0 = Disable transfer from FIFO to DAC. DAC receives code 0 and FIFO is flushed.

Audio 2 Control 2 (7Ah, R/W)

IRQ latch	IRQE enable	DRQ/DACKB enable	Mixer source		FIFO signed mode	FIFO stereo mode	FIFO 16-bit mode
7	6	5	4	3	2	1	0

This register is reset to zero by hardware or software reset.

Bits Definitions:

Bits	Name	Description
7	IRQ latch	Audio 2 Interrupt Request Latch. This latch is set high when the DMA counter rolls over to 0, or when a 1 is written to this bit. The latch is cleared by writing a 0 to this bit or by hardware or software reset.
6	IRQE enable	1 = enable IRQE output for Audio 2. 0 = disable IRQE output for Audio 2.
5	DRQ/ DACKB enable	1 = enable DRQ/DACKB output. Which of pair of is pins enabled, is determined by bits 1:0 of register 7Dh. DRQD/DACKBD is the default. 0 = disable DRQ/DACKB output.
4:3	Mixer source	These bits select the Mixer record source: bit 4 / bit 3 / record source 0 0 playback mixer 0 1 record mixer 1 0 (test) music DAC 1 1 (test) system DAC
2	FIFO signed mode	1 = Audio 2 FIFO 2's complement mode. 0 = Audio 2 FIFO unsigned (offset 8000).
1	FIFO stereo mode	1 = Audio 2 FIFO stereo mode. 0 = Mono data.
0	FIFO 16-bit mode	1 = Audio 2 FIFO 16-bit mode. 0 = Audio 2 FIFO 8-bit mode.

Audio 2 Playback Volume (7Ch, R/W)

Audio 2 volume left				Audio 2 volume right			
7	6	5	4	3	2	1	0

This register controls the playback volume for the second audio channel.

Audio 2 Configuration (7Dh, R/W)

0				FM mix enable	DRQ pull-down enable	DRQ/DACKB select	
7	6	5	4	3	2	1	0

This register is reset to 07h by hardware reset.

Bits Definitions:

Bits	Name	Description
7:4	–	Reserved. Always write 0.
3	FM mix enable	1 = Enable FM mix mode. In this mode the second audio channel is synchronized and added to the FM output (40612.5 Hz). 0 = Disable FM mix mode.
2	DRQ pull-down enable	1 = Enable pull-down on selected DRQ. (reset default) 0 = Disable pull-down on selected DRQ.
1:0	DRQ/ DACKB select	Selects the DRQ/DACKB pairs: bit 1 / bit 0 / DRQ/DACKB 0 0 DRQA/DACKBA 0 1 DRQB/DACKBB 1 0 DRQC/DACKBC 1 1 DRQD/DACKBD

Audio Interrupt Control and Status

Register 7Fh is used to monitor and select audio interrupts. See “Assigning Interrupt Sources” on page 14. This register is meant to replace register B1h.

Interrupt Control and Status (7Fh, R/W)

MPU-401 IRQ	HWV IRQ	Audio 2 IRQ	Audio 1 IRQ	Interrupt select			Output enable
7	6	5	4	3	2	1	0

This register is reset to zero by hardware or software reset. Reading bits 7:4 is a simple way to poll the four interrupt sources.

Bits Definitions:

Bits	Name	Description
7	MPU-401 IRQ	(Read Only) MPU-401 Interrupt Request.
6	HWV IRQ	(Read Only) HW Volume Interrupt Request.
5	Audio 2 IRQ	(Read Only) Audio 2 Interrupt Request.
4	Audio 1 IRQ	(Read Only) Audio 1 Interrupt Request.
3:1	Interrupt select	Interrupt select: bit 3 / bit 2 / bit 1 / interrupt 0 0 0 ES1888 interrupt mode 0 0 1 IRQA 0 1 0 IRQB 0 1 1 IRQC 1 0 0 IRQD 1 0 1 IRQE 1 1 0 Reserved. 1 1 1 Reserved.
0	Output enable	1 = Enable select IRQ output in new interrupt mode. 0 = Disable select IRQ output.

Controller Registers

This is a summary and description of the controller registers. These registers are written to and read from using commands of the format Axh or Bxh. To enable access to these registers send the command C6h.

Table 5 ESS Controller Registers Summary

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Remark
A1h	Clock source	Sample rate divider							S/W reset, unknown
A2h	Filter clock divider								S/W reset, setup for 8 kHz sampling
A4h	2's complement transfer count – low byte								
A5h	2's complement transfer count – high byte								
A8h	0			1	Record monitor enable	0	Stereo/Mono select		Analog Control
A9h	0				1	Microphone preamp enable	0		Mic preamp control
B1h	Game Compatible IRQ	Mask interrupt for DMA transfer complete	Mask interrupt for FIFO half-empty flag transition	Mask all Audio 1 sources	Set to match IRQ select of 7F[3:1]h		x		Legacy audio interrupt control
B2h	DRQ mode	DRQ enable for Extended mode DMA	DRQ enable for Compatibility mode DMA	Inactive DRQ pull-down enable	DRQ/DACKB select		x		Audio DRQ control
B4h	Input volume right				Input volume left				Record volume
B5h	First DMA direct access – low byte								
B6h	First DMA direct access – high byte								
B7h	Enable FIFO to/from CODEC	Set opposite bit 3.	FIFO signed mode	1	FIFO stereo mode	FIFO 16-bit mode	0	Generate load signal	Audio 1 control 1
B8h	0				CODEC mode	DMA mode	DMA read enable	DMA transfer enable	Audio 1 control 2
B9h	0						DMA transfer type select		Audio 1 transfer type

Controller Register Descriptions

Extended Mode Sample Rate Generator (A1h, R/W)

Clock source	Sample rate divider						
7	6	5	4	3	2	1	0

This register should be programmed for the sample rate for all DAC operations in extended mode.

The sample rate is determined by the two's complement divider in bits 7:0.

Sample_Rate = 397.7 kHz / (128-x) if bit 7 = 0.
= 795.5 kHz / (256-x) if bit 7 = 1.

where: x = value in bits 6:0 of register A1h.

Bits Definitions:

Bits	Name	Description
7	Clock source	1 = Clock source is 795.5 kHz for sample rates higher than 22 kHz. 0 = Clock source is 397.7 kHz. for sample rates lower than or equal to 22 kHz.
6:0	Sample rate divider	Signed sample rate divider.

Filter Clock Divider (A2h, R/W)

Filter clock divider							
7	6	5	4	3	2	1	0

This register controls the low-pass frequency of the switch-capacitor filters inside the ES1887. Generally, the filter roll-off should be positioned at 80% – 90% of the Sample_Rate/2 frequency. The ratio of the roll-off frequency to the filter clock frequency is 1:82. In other words, first determine the desired roll-off frequency by taking 80% of the Sample_Rate divided by 2, then multiply by 82 to find the desired Filter Clock frequency. Use the formula below to determine the closest divider:

Filter_Clock_Frequency = 7.16 MHz / (256-Filter_Divider_Register)

Audio 1 Transfer Count Reload (A4h, R/W)

2's complement transfer count – low byte							
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 00h.

Audio 1 Transfer Count Reload (A5h, R/W)

2's complement transfer count – high byte							
7	6	5	4	3	2	1	0

On reset, this register assumes the value of F8h.

The FIFO control logic of the ES1887 has a 16-bit counter for controlling transfers to and from the FIFO. These registers are the re-load value for that counter which is the value that gets copied into the counter after each overflow (plus at the beginning of the initial DMA transfer). The counter will be incremented after each successful byte is transferred via DMA. Since the counter counts up towards FFFF and then overflows, the reload value is in 2's complement form.

For Auto-Initialize DMA, the counter is used to generate interrupt requests to the system processor: in this mode DMA continues indefinitely as far as the ES1887 is concerned. In a typical application the counter is programmed to be one-half of the DMA buffer maintained by the system processor. In this case an interrupt is generated whenever DMA switches from one half of the circular buffer to the other.

For Normal mode DMA, DMA requests will be halted at the time that the counter overflows, until a new DMA transfer is commanded by the system processor. Again, an interrupt request will be generated to the system processor if bit 6 of register B1 is set high.

Analog Control (A8h, R/W)

0			1	Record monitor enable	0	Stereo/Mono select	
7	6	5	4	3	2	1	0

When programming the FIFO for DMA playback modify only bits 1:0. When programming the FIFO for DMA Record modify only bits 3, 1, and 0. Read this register first to preserve the remaining bits.

Bits Definitions:

Bits	Name	Description
7:5	–	Reserved. Always write 0.
4	–	Reserved. Always write 1.
3	Record monitor enable	1 = Enable Record Monitor. 0 = Disable Record Monitor.
2	–	Reserved. Always write 0.
1:0	Stereo/ Mono select	Select operation mode of Audio 1 converters. bit 1 bit 0 Mode 0 0 Reserved 0 1 Stereo 1 0 Mono 1 1 Reserved

Mic Preamp Control (A9h, R/W)

0				1	Microphone preamp enable	0	
7	6	5	4	3	2	1	0

Bits Definitions:

Bits	Name	Description
7:4	–	Reserved. Always write 0.
3	–	Reserved. Always write 1.
2	Mic preamp enable	1 = Enable +26 dB gain in microphone preamp. 0 = Disable +26 dB gain in microphone preamp.
1:0	–	Reserved. Always write 0.

Legacy Audio Interrupt Control B1h

7	6	5	4	3	2	1	0
Game Compatible IRQ	Mask interrupt for DMA transfer complete	Mask interrupt for FIFO half-empty flag transition	Mask all Audio 1 sources	Set to match IRQ select of 7F[3:1]h		x	

Bits Definitions:

Bits	Name	Description
7	Game Compatible IRQ	1 = For Compatibility mode. 0 = For Extended mode.
6	Mask interrupt for DMA transfer complete	1 = Masks the interrupt for Extended mode DMA transfer complete.
5	Mask interrupt for FIFO half-empty flag transition	1 = Masks the interrupt for Extended mode FIFO half-empty flag transition.
4	Mask all Audio 1 sources	1 = Masks all audio 1 sources.
3:2	Set to match IRQ select of 7F[3:1]h	These bits do not select the interrupt pin in New Interrupt method. They should be programmed to match the pin selected by mixer register 7Fh if possible, for those programs that might read the B1h register to determine the interrupt number.

bit 1	bit 0	IRQx Pin	Recommended IRQ
0	0	IRQA	IRQ9
0	1	IRQB	IRQ5
1	0	IRQC	IRQ7
1	1	IRQD	IRQ10

1:0	–	No function.

Audio DRQ Control (B2h, R/W)

DRQ mode	DRQ enable for Extended mode DMA	DRQ enable for Compatibility mode DMA	Inactive DRQ pull-down enable	DRQ/ DACKB select		x	
7	6	5	4	3	2	1	0

On hardware reset, the DRQs are all disabled and the ES1887 microcontroller needs to program the select registers bits 3 and 2. The selected DRQ output is either active or inactive. It is inactive if bits 6:5 are both low.

The inactive DRQ can either be high-impedance or have an active pull-down device, as determined by the value of bit 4 of register B2h. Unless there is a specific reason not to, bit 4 should be set high.

On any reset, all DRQ sources are disabled by clearing bits 7:5.

Bits Definitions:

Bits	Name	Description
7	DRQ mode	1 = For Compatibility mode DRQ. 0 = For Extended mode DRQ.
6	DRQ enable for Extended mode DMA	1 = Enable DRQ outputs and DACKB inputs for DMA transfers in Extended mode. 0 = Enable block I/O to/from the FIFO in Extended mode.
5	DRQ enable for Compatibility mode DMA	1 = Enable DRQ outputs and DACKB inputs for DMA transfers in Compatibility mode. 0 = For Extended mode.
4	Inactive DRQ pull-down enable	1 = Selected DRQ has an active pull-down device. The active pull-down device is required for Compatibility mode to prevent false DRQ requests during the interval between the time that the application programs the system DMA controller and the time the application informs the ES1887 to proceed with DMA. The active pull-down device should be able to sink enough current to override any pull-up device on the system motherboard. It is designed to simulate a resistor < 500 ohms. 0 = Selected DRQ is high-impedance.
3:2	DRQ/ DACK select	DRQ/DACKB select is interpreted as follows:

bit 1	bit 0	DRQx/DACKBx	Suggested Audio 1 DMA
0	0	None	N/A
0	1	DRQA/DACKBA	0
1	0	DRQB/DACKBB	1
1	1	DRQC/DACKBC	3

1:0	–	No function.

Input Volume Control (B4h, R/W)

Input volume left				Input volume right			
7	6	5	4	3	2	1	0

This register controls the stereo input volume controls. Each channel has 4 bits of control, with a resolution of +1.5 dB per step. For recording sources other than the microphone, the input volume varies from -6 dB to +16.5 dB. For the microphone, the input volume varies from +0 dB (no gain) to +22.5 dB. On reset, this register assumes the value of FFh.

First DMA DAC Direct Access (B5h, R/W)

First DMA DAC direct access – low byte							
7	6	5	4	3	2	1	0

Low byte of DAC direct access holding register. Because the bus between the ISA bus and the FIFO is only 8-bits wide, the ES1887 has to have somewhere to hold 16-bit data. Registers B5h and B6h serve this function.

First DMA DAC Direct Access (B6h, R/W)

First DMA DAC direct access – high byte							
7	6	5	4	3	2	1	0

High byte of DAC direct access holding register. Because the bus between the ISA bus and the FIFO is only 8-bits wide, the ES1887 has to have somewhere to hold 16-bit data. Registers B5h and B6h serve this function.

Audio 1 Control 1 (B7h, R/W)

Enable FIFO to/ from CODEC	Set opposite bit 3.	FIFO signed mode	1	FIFO stereo mode	FIFO 16-bit mode	0	Generate load signal
7	6	5	4	3	2	1	0

Bits Definitions:

Bits	Name	Description
7	Enable FIFO to/ from CODEC	1 = Enable Audio 1 FIFO connection to DAC or ADC. This allow transfers to/from the FIFO and the analog circuitry. 0 = Disable Audio 1 FIFO connection to DAC or ADC.
6	Set opposite bit 3.	Reserved function. This bit must be set to the opposite polarity of bit 3, namely high for mono and low for stereo.
5	FIFO signed mode	1 = Audio 1 FIFO 2's complement mode (signed data). 0 = Audio 1 FIFO unsigned (offset 8000).
4	–	Reserved. Always write 1.
3	FIFO stereo mode	1 = Audio 1 FIFO stereo mode. 0 = Audio 1 FIFO mono mode. Bit 6 must be set at the opposite polarity of this bit, namely low for stereo and high for mono.
2	FIFO 16-bit mode	1 = Audio 1 FIFO 16-bit mode. 0 = Audio 1 FIFO 8-bit mode.
1	–	Reserved. Always write 0.
0	Generate load signal	Write 1. Generate a load signal that copies DAC Direct Access Holding register to DAC on the next sample rate clock edge (sample rate is determined by Extended mode register A1h). This bit is cleared after holding register is copied to the DAC.

Audio 1 Control 2 (B8h, R/W)

0				CODEC mode	DMA mode	DMA read enable	DMA transfer enable
7	6	5	4	3	2	1	0

Bits Definitions:

Bits	Name	Description
7:4	–	Reserved. Always write 0.
3	CODEC mode	1 = CODEC in DAC mode. 0 = CODEC in ADC mode.
2	DMA mode	1 = Auto-initialize mode. 0 = normal DMA mode.
1	DMA read enable	1 = Audio 1 is read (e.g., for ADC operation). 0 = Audio 1 is write (e.g., for DAC operation).
0	DMA transfer enable	First DMA active-low reset. When low, the first DMA is held inactive. When high, first DMA is allowed to proceed

Audio 1 Transfer Type (B9h, R/W)

0						DMA transfer type select	
7	6	5	4	3	2	1	0

Bits Definitions:

Bits	Name	Description			
7:2	–	Reserved. Always write 0.			
1:0	DMA transfer type select	Selects the DMA transfer type for the first DMA:			
		bit 1	bit 0	transfer type	bytes/DMA request
		0	0	Single	–
		0	1	Demand	2
		1	0	Demand	4
		1	1	Reserved	–

AUDIO MICROCONTROLLER COMMAND SUMMARY

Table 6 Command Summary

Command	Data Byte(s) Write/Read	Function
10h	1 write	Direct mode 8-bit DAC. Data is 8-bit unsigned format.
11h	2 writes	Direct mode 16-bit DAC. Data is 16-bit unsigned format, first low byte then high byte.
14h	2 writes	Start normal mode DMA for 8-bit DAC transfer. Data is transfer count-1, least byte first. Stereo DAC transfer if Stereo flag is set in Mixer register 0Eh. Maximum sample rate is 44 kHz mono, 22 kHz stereo.
15h	2 writes	Start normal mode DMA for 16-bit DAC transfer. Data is transfer count-1, least byte first. Stereo DAC transfer if stereo flag is set in Mixer register 0Eh. Maximum sample rate is 22 kHz mono, 11 kHz stereo.
1Ch		Start auto-initialize mode DMA for 8-bit DAC transfer. Block size must be previously set by command 48h. Stereo DAC transfer if stereo flag is set in Mixer register 0Eh. Maximum sample rate is 44 kHz mono, 22 kHz stereo.
1Dh		Start auto-initialize mode DMA for 16-bit DAC transfer. Block size must be previously set by command 48h. Stereo DAC transfer if stereo flag is set in Mixer register 0Eh. Maximum sample rate is 22 kHz mono, 11 kHz stereo.
20h	1 read	Direct mode 8-bit ADC. Data is 8-bit unsigned. Firmware-controlled input volume for AGC.
21h	2 reads	Direct mode 16-bit ADC, returns least byte first. Data is 16-bit unsigned format. Input volume controlled via command DDh.
24h	2 writes	Start normal mode DMA for 8-bit ADC transfer. Data is transfer count-1, least byte first. Firmware-controlled input volume for AGC. Maximum sample rate is 22 kHz: use command 99h for higher rates up to 44 kHz.
25h	2 writes	Start normal mode DMA for 16-bit ADC transfer. Data is transfer count-1, least byte first. Input volume controlled via command DDh. Maximum sample rate is 22 kHz.
2Ch		Start auto-initialize mode DMA for 8-bit ADC transfer. Block size must be previously set by command 48h. Firmware-controlled input volume for AGC. Maximum sample rate is 22 kHz: use command 98h for higher rates up to 44 kHz.
2Dh		Start auto-initialize mode DMA for 16-bit ADC transfer. Block size must be previously set by command 48h. Input volume is controlled via command DDh. Maximum sample rate is 22 kHz.
30h/31h		MIDI input mode. Detects MIDI serial input data and transfers to Data register, setting Data Available flag in register Audio_Base+Eh. Command 31h will also generate an interrupt request for each byte received. Exit MIDI input mode by executing a write to port Audio_Base+Ch. The data written is ignored. A software reset will also exit this mode.
34h/35h		MIDI UART mode. Acts like commands 30h/31h, except that any data written to Audio_Base+Ch will be transmitted as MIDI serial output data. The only way to exit this mode is a software reset.
38h	1 write	MIDI output. Transmit one byte.
40h	1 write	Set time constant, x, for timer used for DMA mode DAC/ADC transfers: rate = 1 MHz / (256-x). X must be less than or equal to 233. For stereo transfers, program sample rate for twice the per-channel rate.
41h	1 write	Alternate set time constant, x: rate = 1.5 MHz / (256-x). This command provides more accurate timing for certain rates such as 22,050. X must be less than or equal to 222. For stereo transfers, program sample rate for twice the per-channel rate.
42h	1 write	Set filter clock independently of timer rate. (note that the filter clock is automatically set by commands 40h/41h). Filter clock rate = 7.16E6 / (256-x). The relationship between the low-pass filter -3dB point and the filter clock rate is approximately 1:82.
48h	2 writes	Set block size to -1 for high-speed mode and auto-initialize mode transfer, least byte first.

Table 6 Command Summary (Continued)

Command	Data Byte(s) Write/Read	Function
64h	2 writes	Start ESPCM 4.3-bit (low compression) format DMA transfer to DAC. Data is transfer count-1, least byte first.
65h	2 writes	Same as command 64h, except with reference byte flag.
66h	2 writes	Start ESPCM 3.4-bit (medium compression) format DMA transfer to DAC. Data is transfer count-1, least byte first.
67h	2 writes	Same as command 66h, except with reference byte flag.
6Ah	2 writes	Start ESPCM 2.5-bit (high compression) format DMA transfer to DAC. Data is transfer count-1, least byte first.
6Bh	2 writes	Same as command 6Ah, except with reference byte flag.
6Eh	2 writes	Start ESPCM 4.3-bit (low compression) format ADC, compression, and DMA transfer. Data is transfer count-1, least byte first.
6Fh	2 writes	Same as command 6Eh, except with reference byte flag.
74h	2 writes	Start ADPCM 4-bit format DMA transfer to DAC. Data is transfer count-1, least byte first.
75h	2 writes	Same as command 74h, except with reference byte flag.
76h	2 writes	Start ADPCM 2.6-bit format DMA transfer to DAC. Data is transfer count-1, least byte first.
77h	2 writes	Same as command 76h, except with reference byte flag.
7Ah	2 writes	Start ADPCM 2-bit format DMA transfer to DAC. Data is transfer count-1, least byte first.
7Bh	2 writes	Same as command 7Ah, except with reference byte flag.
80h	2 writes	Generate silence period. Data is number of samples-1.
90h		Start auto-initialize, DMA 8-bit transfer to DAC. Transfer count must be previously set by command 48h.
91h		Start DMA 8-bit transfer to DAC. Transfer count must be previously set by command 48h.
98h		Start high-speed mode, auto-initialize, DMA 8-bit transfer from ADC. Transfer count must be previously set by command 48h. There is no AGC. Input volume is controlled with command DDh. Maximum sample rate is 44 kHz.
99h		Start high-speed mode, DMA 8-bit transfer from ADC. Transfer count must be previously set by command 48h. There is no AGC. Input volume is controlled with command DDh. Maximum sample rate is 44 kHz.
Axh, Bxh, Cxh		(where x = 0 to Fh) ES1887 extension commands. Many of these commands are used to access the ES1887's controller registers. For information on these registers, see the register descriptions.
C0h		Read controller register.
C1h		Resume after suspend.
C6h		Enable ES1887 Extension commands Ax, Bx. Must be issued after every reset.
C7h		Disable ES1887 Extension commands Ax, Bx.
CEh	1 read	Read GPO0/1 Power Management Register.
CFh	1 write	Write GPO0/1 Power Management Register.
D0h		Pause DMA. Internal FIFO operations will continue until the FIFO is empty (DAC transfer) or full (ADC transfer). It is not necessary to use this command to stop DMA if the transfer is completed normally and the end-of-DMA interrupt is generated.
D1h		Enable Audio 1 DAC input to playback mixer.
D3h		Disable Audio 1 DAC input to playback mixer.
D4h		Continue DMA after command D0h.

Table 6 Command Summary (Continued)

Command	Data Byte(s) Write/Read	Function
D8h	1 read	Return Audio 1 DAC enable status: 0=disabled FFh=enabled
DCh	1 read	Return current input gain, 0-15 (valid during 16-bit ADC and 8-bit “high-speed mode” ADC).
DDh	1 write	Write current input gain, 0-15 (valid during 16-bit ADC and 8-bit “high-speed mode” ADC).
E1h	2 reads	Return version number high (3), followed by version number low (1). This indicates Sound Blaster Pro compatibility.
E7h	2 reads	Returns Legacy ES688/ES1688 identification bytes: 68h 8xh, where x is the version code. This command may cause other sound card to perform an unknown function, in which case the sound card should be reset after this command is used. The version code, x, is less than 8 for the ES688 and greater than or equal to 8 for the ES1688. See “Identifying the ES1887” on page 28.
F2h		Generate an interrupt for test purposes.
FDh		Forces power-down. Software or hardware reset is required for wake-up.

POWER MANAGEMENT

The ES1887 has three power states:

- full power-up
- partial power-down
- full power-down

The decision to power-down partially or fully is made by the system processor. To assist the system processor, activity flags are available that can be monitored by the system processor to track I/O activity to and from the ES1887. After a predetermined idle period, the ES1887 can be commanded to power-down partially or fully.

If the oscillator clock is provided from an external circuit, automatic wake-up upon I/O activity is available. With this feature, the act of reading or writing to an ES1887 I/O port causes the chip to immediately power-up without losing context from partial or fully powered-down states.

If the oscillator clock is provided by a crystal, automatic wake-up from partial power-down is still available because the oscillator continues to run as long as the ES1887 is not fully powered-down. Once the chip is fully powered-down, however, automatic wake-up is not available with a crystal oscillator because of the start-up requirements of the crystal oscillator. It is then the responsibility of the system software to provide for a start-up period for the oscillator before returning control to the application programs that may access the ES1887. In any case, there is no loss of context.

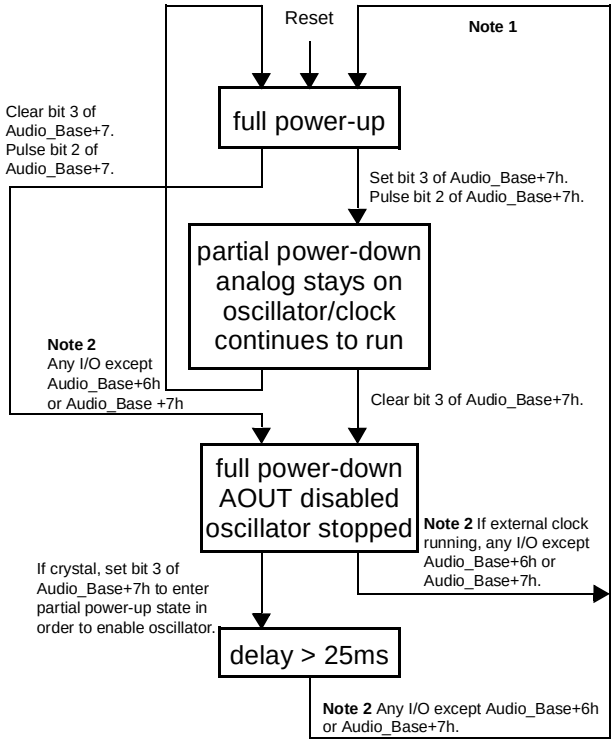


Figure 1 Summary of power states in the ES1887

Note 1: after return to full power-up state from full power-down state, the AOUT L/R analog output pins will not be enabled for 48 to 64 msec. The chip should remain in the full power-up state for at least 64 msec to be sure the AOUT pins are enabled before changing to the partial power-down state. Otherwise the AOUT pins may never get enabled. For this reason it is not possible to go directly from full power-down to partial power-down and have AOUT enabled.

Note 2: a Low input on any of the three hardware volume control pins (VOLUP, VOLDN, or MUTE) will also act as a wake-up event.

State	Description	Notes
0	Full power-down. Crystal oscillator disabled. AOUT_L and AOUT_R held at approximately CMR by high value resistors.	All inputs static at VDDD or GND.
1	Partial power-down. Joystick, MPU-401 are up. Audio, FM, ES689/ES69x interface, and DSP serial interface are down.	Digital standby.
2	Full power-up. This is the state after hardware reset.	Normal operating conditions.

Partial Power-Down

In the partial power-down state, the power supply remains connected to the chip during power-down and the chip's analog section remains active while the digital circuits are mostly inactive.

The total current used by the ES1887 can be reduced by a factor of two or more by putting the ES1887 in a partial power-down state. The crystal oscillator, if used, continues to operate. The analog circuitry remains powered-up so that AuxA, AuxB, Line, and Mic audio sources can continue to be heard. FM and digital audio are muted. There should be no pop when returning from partial power-down to a full power-up state.

The following items are effective for partial power-down operation:

- Oscillator is enabled.
- MPU-401 operates.
- Configuration device operates.
- H/W volume operates.
- Mixer operates.
- Analog operates.
- Joystick operates.
- Audio device is disabled, FM disabled.
- Auto wake-up with any I/O activity to FM or audio registers except Audio_Base+4h, Audio_Base+5h, Audio_Base+6h, Audio_Base+7h.

Causing Partial Power-Down

To cause the partial power-down state, bit 3 of register Audio_Base+7h must be high before pulsing bit 2 high, then low, and bit 3 must remain high.

Example: powering down the ES1887 using system software timer interrupt

In this example, it is assumed that the ES1887 is not using a crystal for its clock.

From a timer interrupt routine, read Audio_Base+6h to monitor activity. After one minute of I/O inactivity, you decide to power-down the ES1887 completely, and then return from the timer interrupt. The ES1887 will wake up automatically upon any I/O access to the ES1887 by any application.

1. Check if the ES1887 is already powered down (bit 3 of port Audio_Base+6h = 0). If so, there is nothing to do.
2. Check if the ES1887 is being held in reset by reading bit 0 of port Audio_Base+6h. If bit 0 is high, release the reset before powering-down: Clear bit 0 of port Audio_Base+6h, then delay 1 msec or more for the ES1887 microcontroller to complete its initialization.
3. Check if the ES1887 is in MIDI mode by testing bit 2 of port address Audio_Base+6h. While the ES1887 can power-down when in MIDI mode, it will not automatically wake-up if serial data comes in to the MSI pin, and such data will be lost.
4. Send a power-down request to the chip by clearing bit 3 in register Audio_Base+7h, then pulsing bit 2 first high, then low. The other bits of this register should be preserved. The ES1887 microcontroller sees the rising edge of bit 2 of register Audio_Base+7h as an interrupt request to power-down.

Waking from Partial Power-down

Any I/O activity, except Audio_Base+6h or Audio_Base+7h, will wake the ES1887 from a partial power-down.

Full Power-Down

Complete power-down reduces the operating current to less than 50 microamps.

The following items are indicators of a full power-down operation:

- Nothing operates, except for some programmed I/O.
- The Activity Flags from a Port Audio_Base+6h Read are:
  - Bit 7 Activity latch Joystick, MPU-401, Config, or DMA activity.
  - Bit 6 Activity latch: Audio_Base+4h, Audio_Base+5h I/O.
  - Bit 5 Activity latch: Audio (except Audio_Base+4h, Audio_Base+5h, Audio_Base+6h read, Audio_Base+7h read/write), FM I/O or DMA.
  - Bit 4 DSP and ES689/ES69x serial activity status.

Waking from Full Power-Down

There are three main ways to wake the chip up from full power-down:

- Hardware reset
- Software reset
- I/O activity

Hardware or Software Reset

The chip is automatically restored to activity upon a hardware reset. Context is not preserved.

I/O Activity Causing Automatic Wake-up

Automatic wake-up is the method whereby the chip returns to the full power-up state, triggered by I/O activity. With automatic wake-up the context is preserved.

Any I/O access to any of the ES1887 port addresses other than Audio_Base+6h or Audio_Base+7h causes an automatic wake-up.

Auto wake-up is also triggered by DMA accesses. However, it is unlikely this will occur if power-down is triggered by a period of I/O inactivity, which includes DMA accesses and the I/O operations required to set up the DMA transfer.

Automatic wake-up requires that XI is driven by a stable clock. This can either be an external clock source or from a crystal. In the latter case, automatic wake-up of the ES1887 is not supported. This is because the oscillator requires some time (typically greater than 25 msec) to stabilize.

In the full power-down state the oscillator is stopped and the analog circuitry is powered-down. The AOUT_L and AOUT_R pins are left at approximately the reference voltage by a high-impedance resistor divider.

To wake the chip from a full power-down, set bit 3 of port Audio_Base+7h high for 25 msec, to enter the partial power-down state. Any I/O activity, except Audio_Base+6h or Audio_Base+7h, will then wake the ES1887 from a partial power-down.

Inputs and Outputs During Power-Down

When powered-down, digital inputs that do not have pull-up or pull-down devices should be driven high or low, that is, they should not be floating. Examples of such pins are A[11:0] and AEN.

Some input pins have circuitry that provides a pull-down device when the ES1887 digital circuits are powered up. During power-down, these inputs have a feedback device that latches the input state and prevents leakage current into the pin. The pull-down device is disabled.

The pins that have this feature are: AMODE, SE, DR

Output pins such as DRQx and IRQx are frozen in their state at power-down.

GPO0 and GPO1 can change state during full power-down if so programmed (see “General-Purpose Outputs and Power-Down” on page 26).

The MSI pin has an internal pull-up device, so this pin can be left floating during power-down.

The internal inverter connected to pins XI and XO continues to operate when the digital part of the ES1887 is powered-down as long as the analog part of the ES1887 is powered-up

When the chip is fully powered-down, the inverter becomes high-impedance with a weak pull-up on the XO pin.

VREF goes low when the analog circuitry is powered-down.

CMR is pulled low by an internal transistor during analog power-down.

The AOUT_L and AOUT_R pins are held at approximately the idle voltage level with a high-impedance resistor divider. After return to full power-up state from full power-down state, the AOUT analog output pins aren’t enabled for 48 to 64 msec. Keep the chip in the full power-up state for at least 64 msec to be sure the AOUT pins are enabled before changing to the partial power-down state. Otherwise the AOUT pins may never get enabled. For this reason, it is not possible to go directly from full power-down to partial power-down and have AOUT enabled.

Suspend/Resume

In Suspend/Resume, power is removed from the ES1887 during its suspended state. Before removing power, the entire context of the microcontroller and registers must be uploaded to the system processor and saved. After restoring power and generating a hardware reset, the opposite resume operation downloads the context.

The term “suspend” is used here to describe the process of uploading the context of the ES1887 and removing digital and analog power to the chip. The term “resume” describes the process of applying power to the ES1887 and downloading the context.

The ES1887 requires 782 bytes to store its entire context.

It is possible to suspend the ES1887 regardless of its current state. This includes suspending in the middle of a DMA transfer.

To suspend operation of the ES1887 pulse bit 7 of port address Audio_Base+7h high, then low. This interrupts the ES1887 microcontroller and begins a sequence of upload operations.

To resume operation of the ES1887, a hardware reset is required before downloading the context. Downloading the context is initiated with command C1h. Before sending the download command send the C6h command to enable access to the Extension commands.

A sample assembly language program that implements Suspend/Resume from a TSR is available from the Applications Department of ESS Technology, Inc.

Pop Prevention in the External Amplifier

Normally, in order to directly drive speakers in an ES1887 design, an external stereo amplifier chip is used. There are two power management problems associated with an external amplifier:

1. The amplifier itself draws current unless it can be powered down.

2. Suspend/Resume causes pops because power is removed from the ES1887 and then re-applied.

Amplifiers such as the SGS/Thomson TDA7233 have a mute input which reduces current to 400 µa and also reduces pops from the suspend/resume process. This part is a mono amplifier, so two are required. Connect GPO0 to the active-low MUTE input of the TDA7233. In this case the amplifier is muted after hardware reset. During start-up, program the ES1887 so that GPO0 is high when powered-up and low when fully powered-down. Program a delay of about 133 msec between power-down and power-up states, before GPO0 returns high so that the ES1887 analog circuits can settle.

Power Management and the FM Synthesizer

The ES1887 FM synthesizer is a fully static design. This means that the clock can be stopped to power-down the circuitry without loss of state. For suspend/resume applications, the entire context of the synthesizer can be read back.

Self-Timed Power-Down

The ES1887 microcontroller can be programmed to monitor I/O activity in place of the system processor, and after a programmable period of inactivity, enter either a partial or full power-down state.

In Self-Timed Power-Down mode, power is maintained as for partial or full power-down, except the decision to power-down is made by the ES1887 itself. The ES1887 microcontroller waits for a pre-programmed period of I/O inactivity between successive commands, before entering partial or full power-down state.

The ES1887 needs to use the activity flags in port Audio_Base+6h. Therefore, if this feature is enabled, the system processor can't monitor I/O activity.

Enabling Self-Timed Power-Down

1. Send command C6h to enable access to the controller registers.
2. Send command BDh.
3. Send the time out value N, where the time period is N x 8 seconds. If N is zero, self-timed power-down is disabled.
4. Send command C7h to disable access to the controller registers.

Whether the ES1887 enters partial or full power-down is determined by bit 3 of register Audio_Base+7h.

Even if self-timed power-down is enabled, the ES1887 can be commanded to power-down via bit 2 of register Audio_Base+7h.

There is one limitation to this feature: the timing of inactivity only occurs between commands sent to the ES1887. It is possible for a program to leave the ES1887 in a state where timing doesn't happen. For example, if a program exits without a DMA transfer being completed. Most programs are well-behaved in this respect and leave the ES1887 in a well defined state.

General-Purpose Outputs and Power-Down

The ES1887 has the ability to have one or both of the general-purpose outputs GPO0 and GPO1 change state when the ES1887 is powered-down.

After hardware reset, this feature is disabled and the general-purpose outputs are not affected by power-down. A controller register in the ES1887 must be programmed to enable this feature. Specifically, the GPO power-down control register is set by writing the command CFh to port Audio_Base+Ch followed by the data. To read the GRO power-down controller register write the command CEh to Audio_Base+Ch and read the data from port Audio_Base+Ah. This register should be set once by system software after system reset. This register is unaffected by soft resets. Using this register, one or both of the general-purpose outputs can be programmed to be inverted from their normal state during power-down. The normal state of each pin is set by the appropriate bits 1:0 of port Audio_Base+7h. A further feature allows the inverted outputs to return to their normal state immediately after power-up or after a programmed delay after power-up.

GPO Power-Down Register

Delay GPO0 state return enable	1: invert GPO1 at power-down	Delay GPO0 state return enable	1: invert GPO0 at power-down	0	Time delay		
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 00h. This means that GPO0 and GPO1 are unaffected by the power-down status; that is, they remain in the state programmed into port Audio_Base+7h.

NOTE: "Power-down" as used in this document refers to full power-down, i.e., when both the analog and digital parts of the ES1887 are powered-down.

Bits Definitions:

Bits	Name	Description
7	Delay GPO1 state return enable	1 = Delay GPO1's return to its normal state as determined by port Audio_Base+7h bit 1. The time delay is determined by bits 2:0, described below. 0 = Return GPO1 to its normal state immediately upon wake-up from full power-down.
6	GPO1 invert enable	1 = invert bit 1 of Audio_Base+7h when entering the full power-down state.
5	Delay GPO0 state return enable	1 = Delay GPO0's return to its normal state as determined by port Audio_Base+7h bit 0. The time delay is determined by bits 2:0, described below. 0 = Return GPO0 to its normal state immediately upon wake-up from full power-down.
4	GPO1 invert enable	1 = invert bit 0 of Audio_Base+7h when entering the full power-down state.
3	–	Reserved. Always write 0.
2:0	Time delay	The time period is determined by bits [2:0]: A 16 Hz counter starts at 0 and counts until it equals the 3-bit number "time delay". The maximum delay is (Time delay = 7) times (67 msec) or about 469 msec.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Ratings	Symbol	Value	Units
Analog supply voltage range	VDDA	-0.3 to 7.0	V
Digital supply voltage range	VDDD	-0.3 to 7.0	V
Input voltage	VIN	-0.3 to 7.0	V
Operating temperature range	TA	0 to 70	°C
Storage temperature range	TSTG	-50 to 125	°C

WARNING: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. There are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Thermal Characteristics

The ES1887 is designed to operate at case temperatures less than 78º C.

Operating Conditions

The ES1887 digital and analog characteristics operate under the following conditions:

VDDD	4.5V to 5.5V
VDDA	4.75V to 5.25V
TA	25°

Table 7 Digital Characteristics

Parameter	Symbol	Min	Max	Unit (conditions)
Input high voltage: all inputs except XI.	VIH1	2.0		Volts (VDDD = min)
Input high voltage: XI.	VIH2	3.0		Volts (VDDD = min)
Input low voltage	VIL		0.8	Volts (VDDD = max)
Output low voltage: all outputs except D[15:0], IRQ(A-E), DRQ(A-D)	VOL1		0.4	Volts (IOL = 4 mA, VDDD = min)
Output high voltage: all outputs except D[15:0], IRQ(A-E), DRQ(A-D)	VOH1	2.4		Volts (IOH = -3 mA, VDDD = max)
Output low voltage: D[15:0], IRQ(A-E), DRQ(A-D)	VOL2		0.4	Volts (IOL = 16 mA, VDDD = min)
Output high voltage: D[15:0], IRQ(A-E), DRQ(A-D)	VOH2	2.4		Volts (IOH = -12 mA, VDDD = max)
Output low voltage	VOL3		0.4	Volts (IOL = 0.8 mA)
VDDD active	ICC1		60	mA (VDDD = max osc. rate at 14.32 MHz)
VDDA active	ICC2		40	mA (VDDA = max)

Table 8 Analog Characteristics

Parameter	Pins	Min	Typ	Max	Unit (conditions)
Reference voltage	CMR, VREF		2.25		volts (VDDA = 5.0V)
Input impedance	LINE_L, LINE_R, AUXA_L, AUXA_R, AUXB_L, AUXB_R, MIC	30k		100k	ohms
	CIN_L, CIN_R	35k	50k	65k	ohms
Output impedance	FOUT_L, FOUT_R	3.5k	5k	6.5k	ohms
	AOUT_L, AOUT_R max load for full-scale output range		5k		ohms
Input voltage range	MIC	10		125	mVp-p
	LINE_L, LINE_R, AUXA_L, AUXA_R, AUXB_L, AUXB_R	0.5		VDDA -1.0	volts
Output voltage range	AOUT_L, AOUT_R max load for full-scale output range	0.5		VDDA -1.0	volts
Mic preamp gain	MIC		26		decibels (dB)

ES1887 TIMING DIAGRAMS

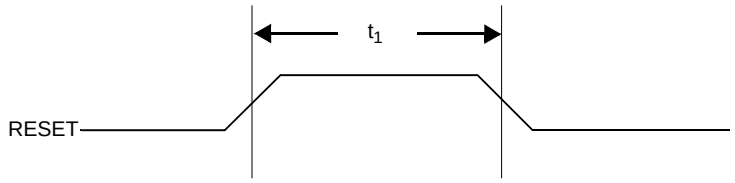


Figure 2 Reset Timing

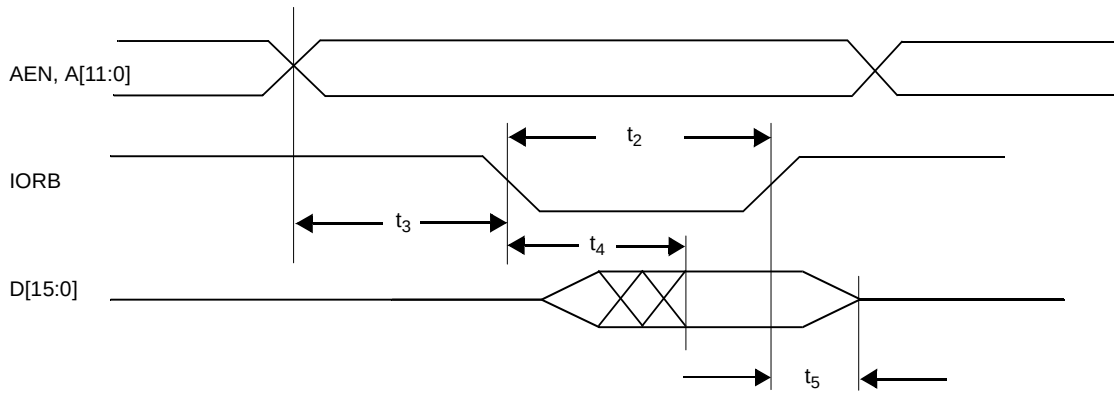


Figure 3 I/O Read Cycle

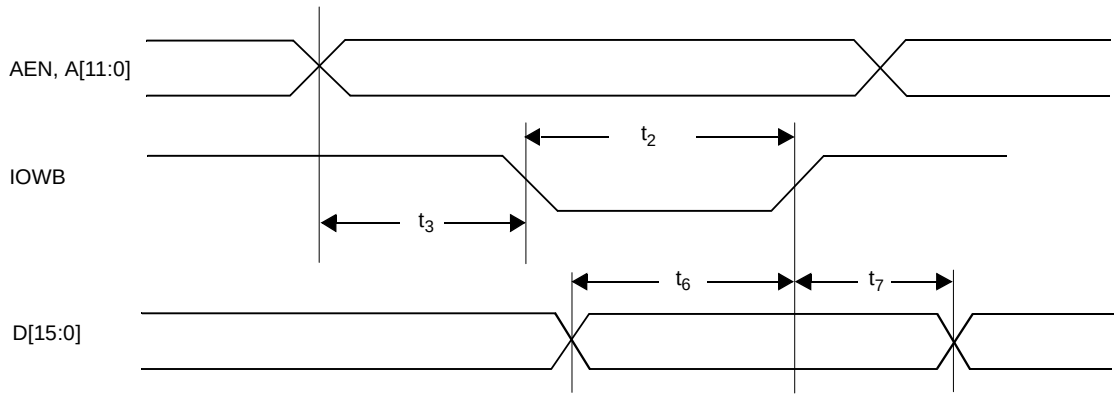


Figure 4 I/O Write Cycle

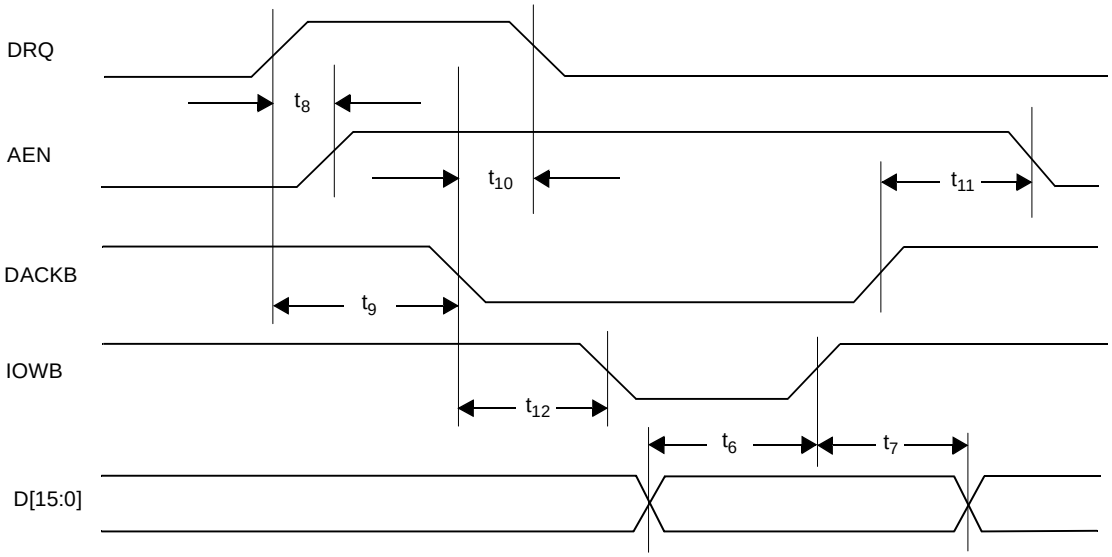


Figure 5 Compatibility Mode DMA Write Cycle[1]

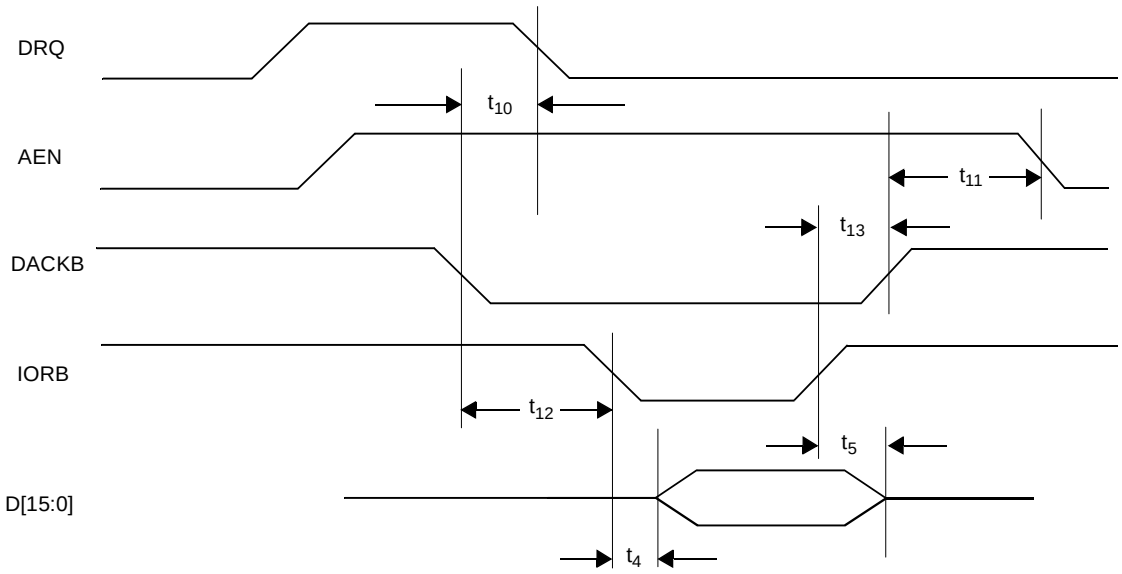


Figure 6 Compatibility Mode DMA Read Cycle[1]

1. In Compatibility mode DMA, the DMA request is reset by the acknowledge signal going low. In Extended mode DMA, the DMA request is reset when the acknowledge signal is low AND the correct command signal is low – either IORB (for DMA read from I/O device) or IOWB (for DMA write to I/O device). For Extended mode DMA, the time t_{10} is relative to the later of the falling edge of the acknowledge signal or the command signal.

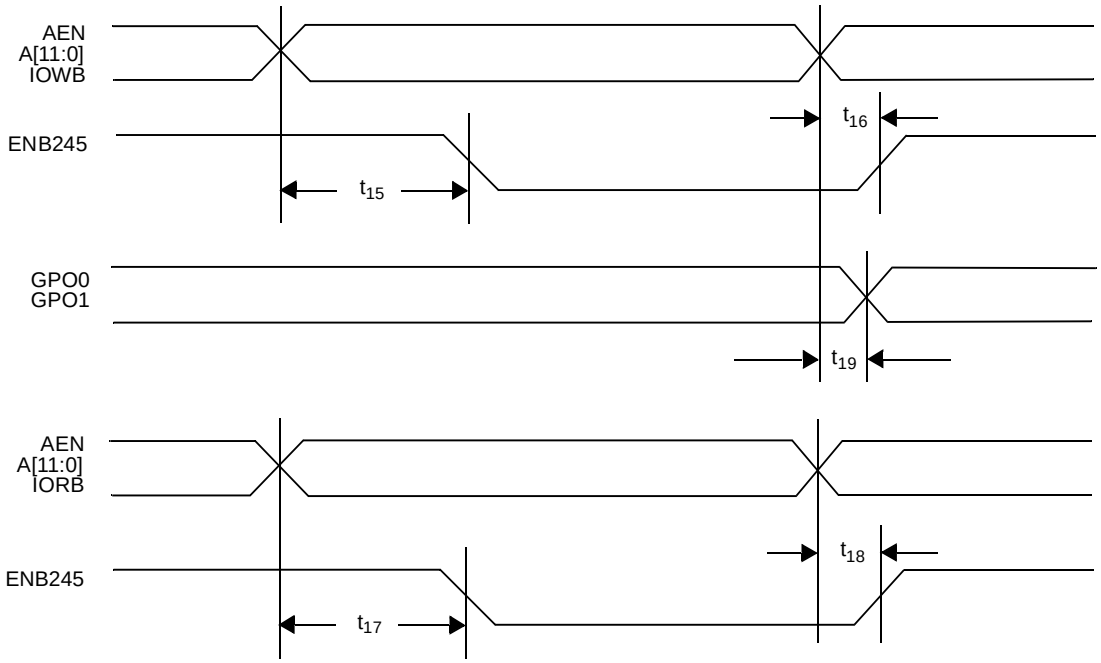


Figure 7 Miscellaneous Output Signals

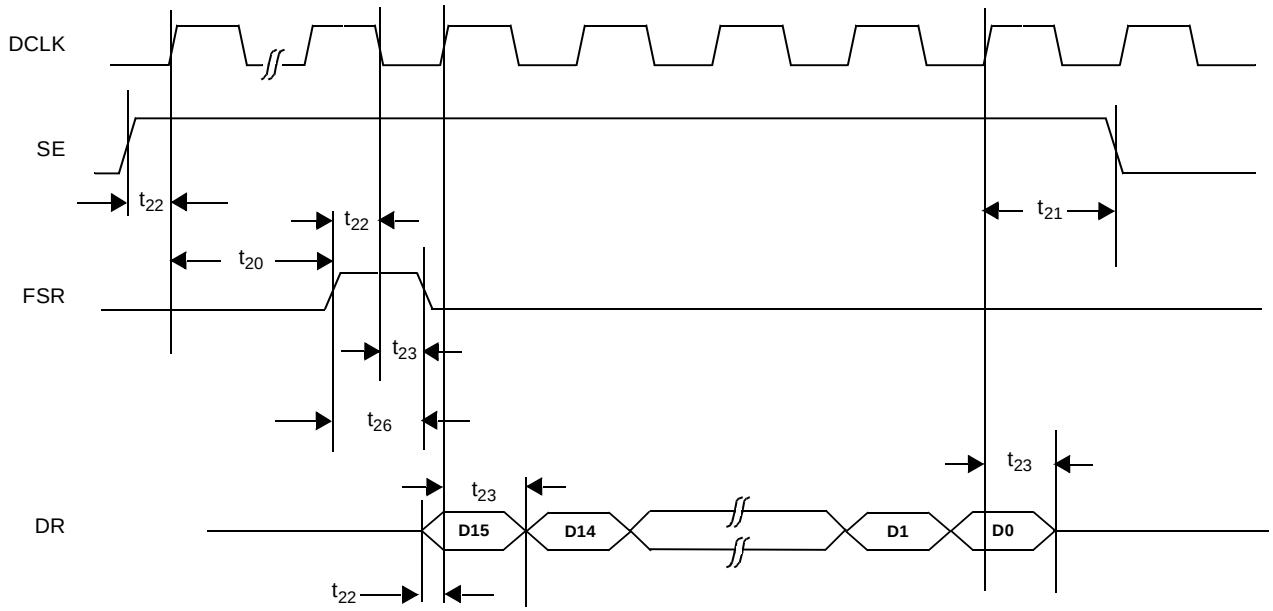


Figure 8 Serial Mode Receive Operation

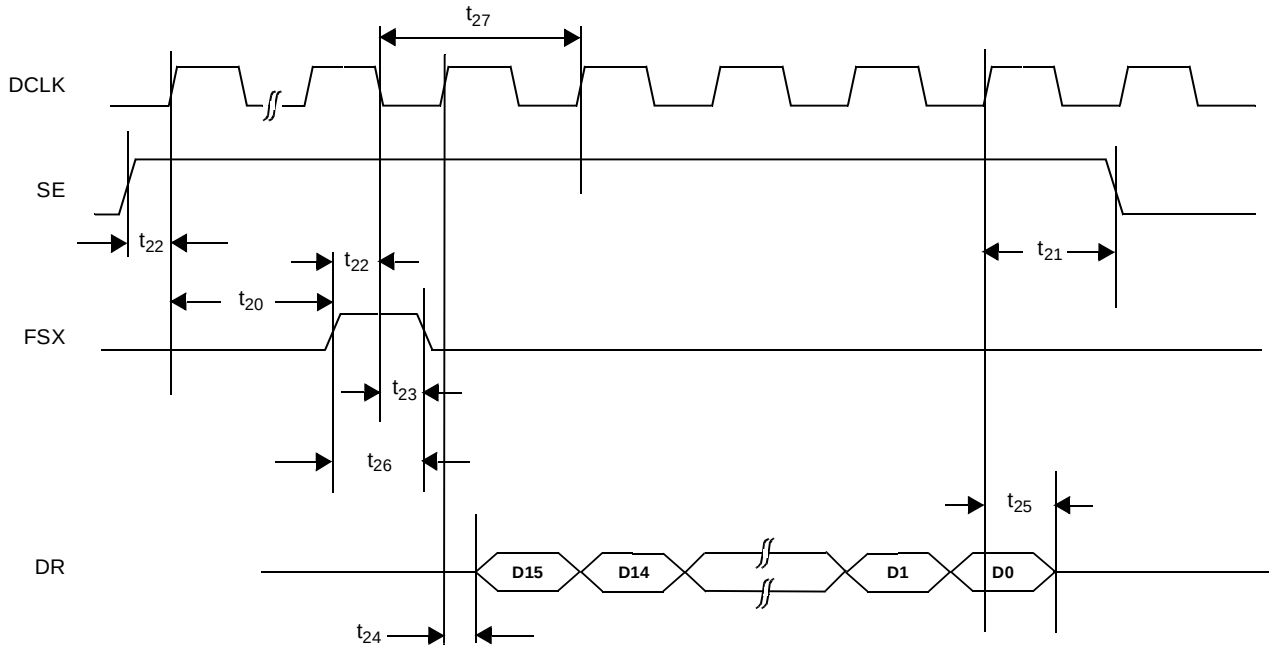


Figure 9 Serial Mode Transmit Operation

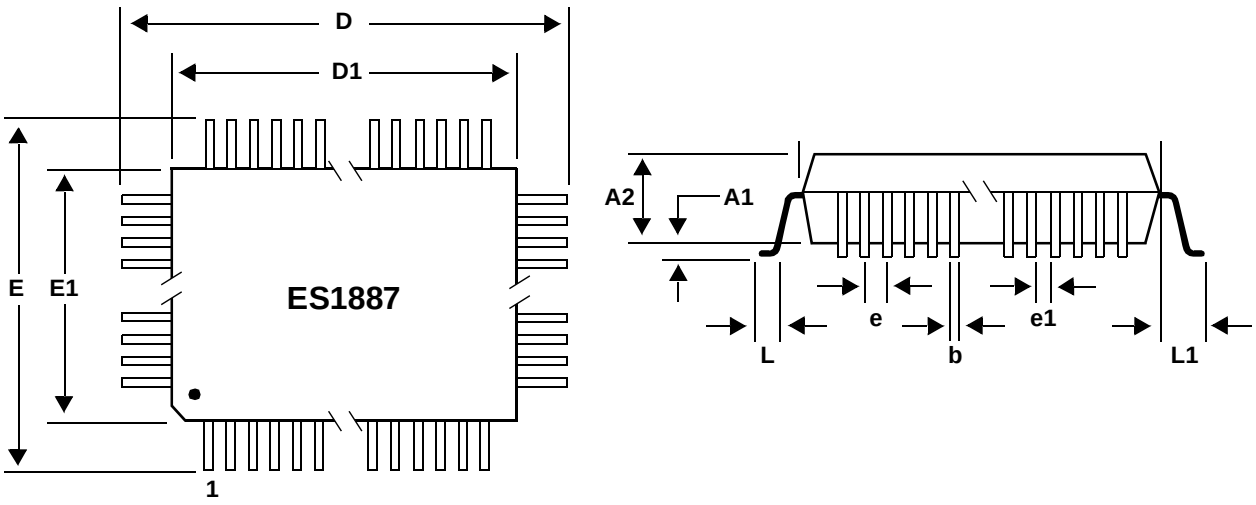
TIMING CHARACTERISTICS

Table 9 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_1	Reset pulse width	300			ns
t_2	IORB, IOWB pulse width	100			ns
t_3	IORB, IOWB address setup time	10			ns
t_4	Read data access time			70	ns
t_5	Read data hold time			10	ns
t_6	Write data setup time	5			ns
t_7	Write data hold time	10			ns
t_8	DMA request to AEN high	0			ns
t_9	DMA request to DMA ACK	10			ns
t_{10}	DMA ACK to request release[a]			30	ns
t_{11}	DMA ACK high to AEN low	0			ns
t_{12}	DMA ACK to IOWB, IORB low	0			ns
t_{13}	IOWB, IORB to DMA ACK release	20			ns
t_{14}	Crystal frequency, XI/XO		14.318		MHz
t_{15}	AEN, A[11:0], IOWB to ENB245 low			20	ns
t_{16}	AEN, A[11:0], IOWB to ENB245 high			15	ns
t_{17}	AEN, A[11:0], IORB to ENB245 low			25	ns
t_{18}	AEN, A[11:0], IORB to ENB245 high			25	ns
t_{19}	AEN, A[11:0], IOWB, IORB to GPO0, GPO1 delays			20	ns
t_{20}	SE high to valid FSR, FSX edge	2			DCLK
t_{21}	SE release time to last DX, DR data bit	1			DCLK
t_{22}	SE, FSX, FSR setup time to DCLK edge	15			ns
t_{23}	SE, FSX, FSR, DR hold time to DCLK edge	10			ns
t_{24}	DX delay time from DCLK edge			20	ns
t_{25}	DX hold time from DCLK edge	10			ns
t_{26}	FSR, FSX pulse width	60	500		ns
t_{27}	DCLK clock frequency		2.048		MHz

a. In Compatibility mode DMA, the DMA request is reset by the acknowledge signal going low. In Extended mode DMA, the DMA request is reset when the acknowledge signal is low AND the correct command signal is low – either IORB (for DMA read from I/O device) or IOWB (for DMA write to I/O device). For Extended mode DMA, the time t_{10} is relative to the later of the falling edge of the acknowledge signal or the command signal.

MECHANICAL DIMENSIONS



Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	23.65	23.90	24.15
D1	Package's outside, X-axis	19.90	20.00	20.10
E	Lead to lead, Y-axis	17.65	17.90	18.15
E1	Package's outside, Y-axis	13.90	14.00	14.10
A1	Board standoff	0.10	0.25	0.36
A2	Package thickness	2.57	2.71	2.87
b	Lead width	0.20	0.30	0.40
e	Lead pitch	-	0.65	-
e1	Lead gap	.24	-	-
L	Foot length	0.65	0.80	0.95
L1	Lead length	1.88	1.95	2.02
-	Foot angle	0º	-	7º
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	30	-
-	Leads in Y-axis	-	20	-
-	Total leads	-	100	-
-	Package type	-	PQFP	-

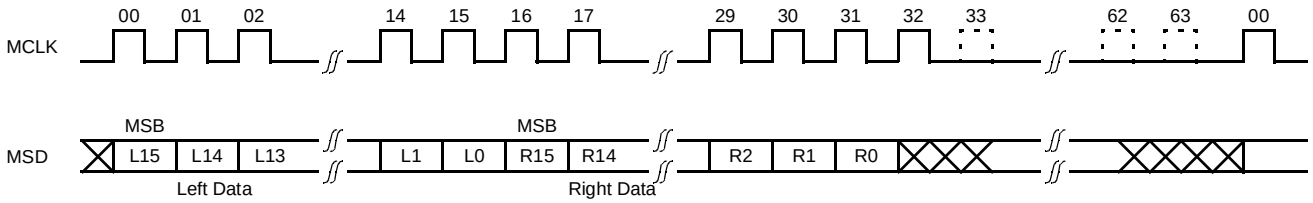
Figure 10 Mechanical Dimensions

APPENDIX A: ES689/ES69X DIGITAL SERIAL INTERFACE

In order for the ES689/ES69x to acquire the FM DAC, bit 4 of Mixer register 48h inside the ES1887 must be set high. When bit 4 is set high, activity on the MCLK signal will cause the FM DAC to be connected to the ES689/ ES69x. If MCLK stays low for more than a few sample periods the ES1887 will reconnect the FM DAC to the FM synthesizer.

After reset, the ES689/ES69x will transmit samples continuously. In this mode bit 4 of Mixer register 48h must be set/cleared to assign the current owner of the FM DAC.

The ES689/ES69x can be programmed to enter Activity-Detect mode using system exclusive command 4. In this mode, the ES689/ES69x will block the serial port output (i.e., set MSD and MCLK low) if no MIDI input is detected on the MSI pin for a period of 5 seconds. It will resume output of data on the serial port as soon as a MIDI input is detected on the MSI pin. This is the recommended mode of operation.



Bit Clock Rate (MCLK): 2.75 MHz

Sample Rate: 42968.75 Hz

MCLK Clocks per Sample:33 clocks (+ 31 missing clocks)

MSD Format:16 bits, unsigned (offset 8000h), MSB first

MSD changes after rising edge of MCLK. Hold time relative to MCLK rising edge is 0-25 nanoseconds.

APPENDIX B: SCHEMATIC EXAMPLES

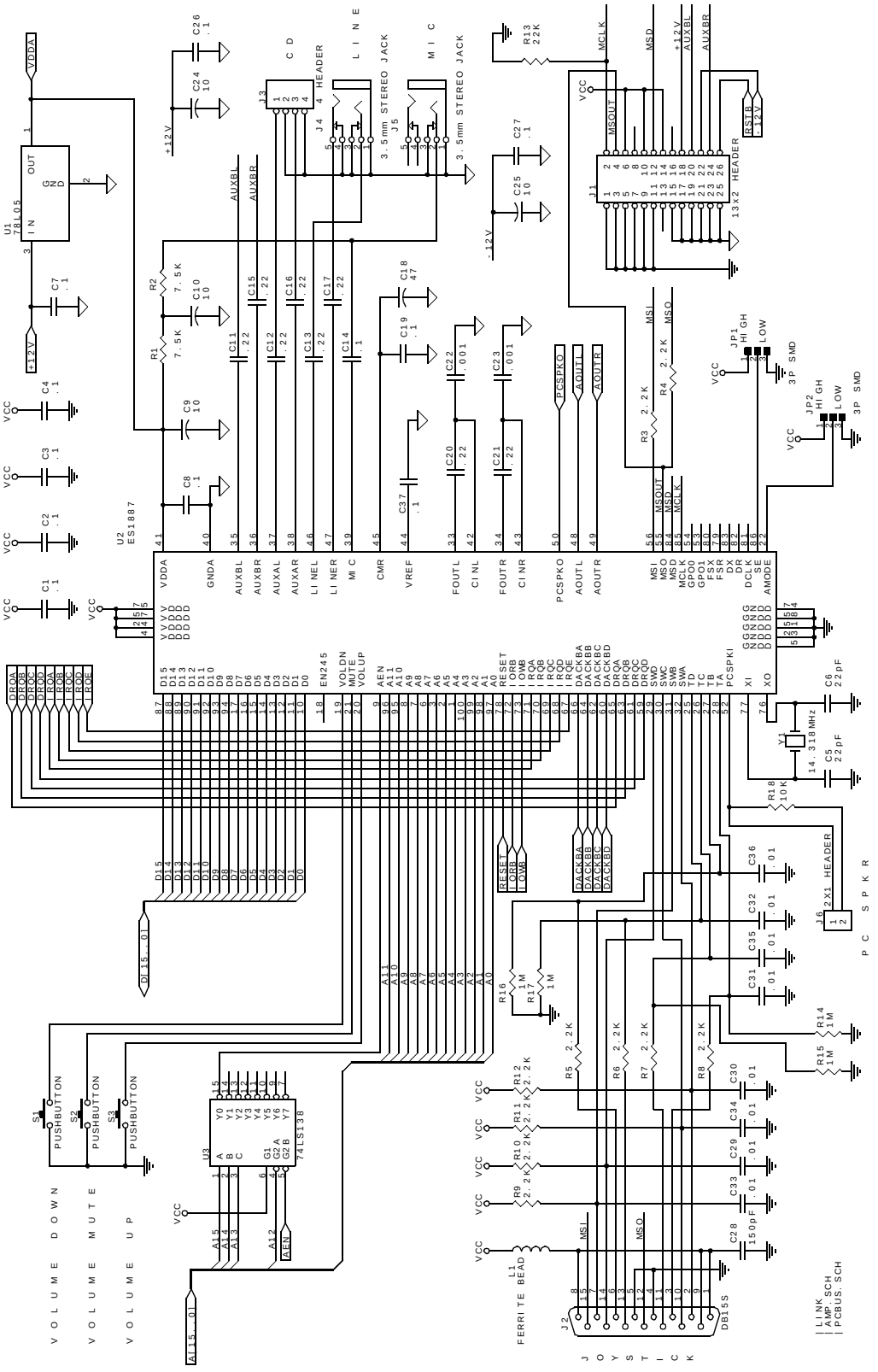


Figure 11 ES1887

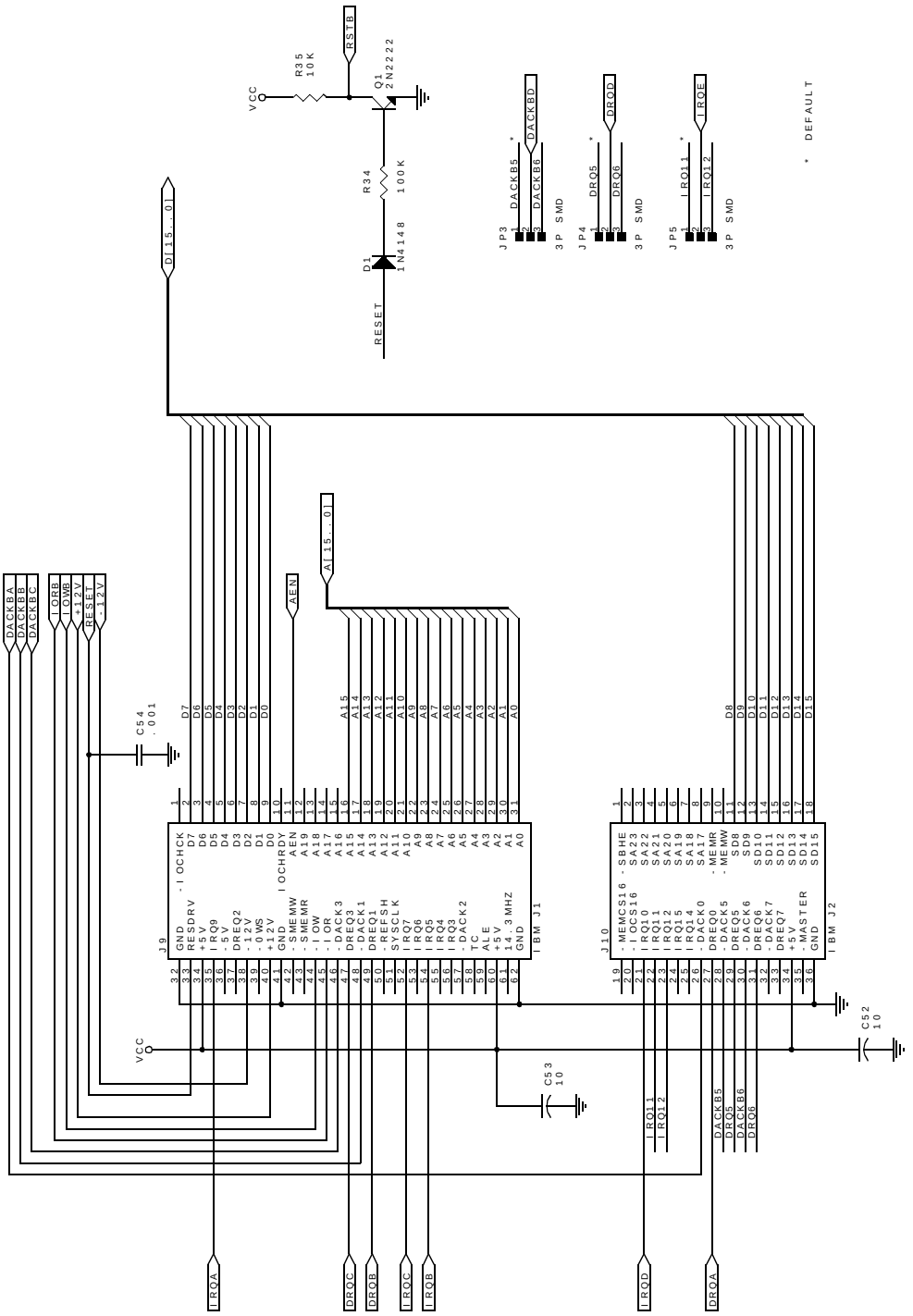


Figure 12 PC Interface

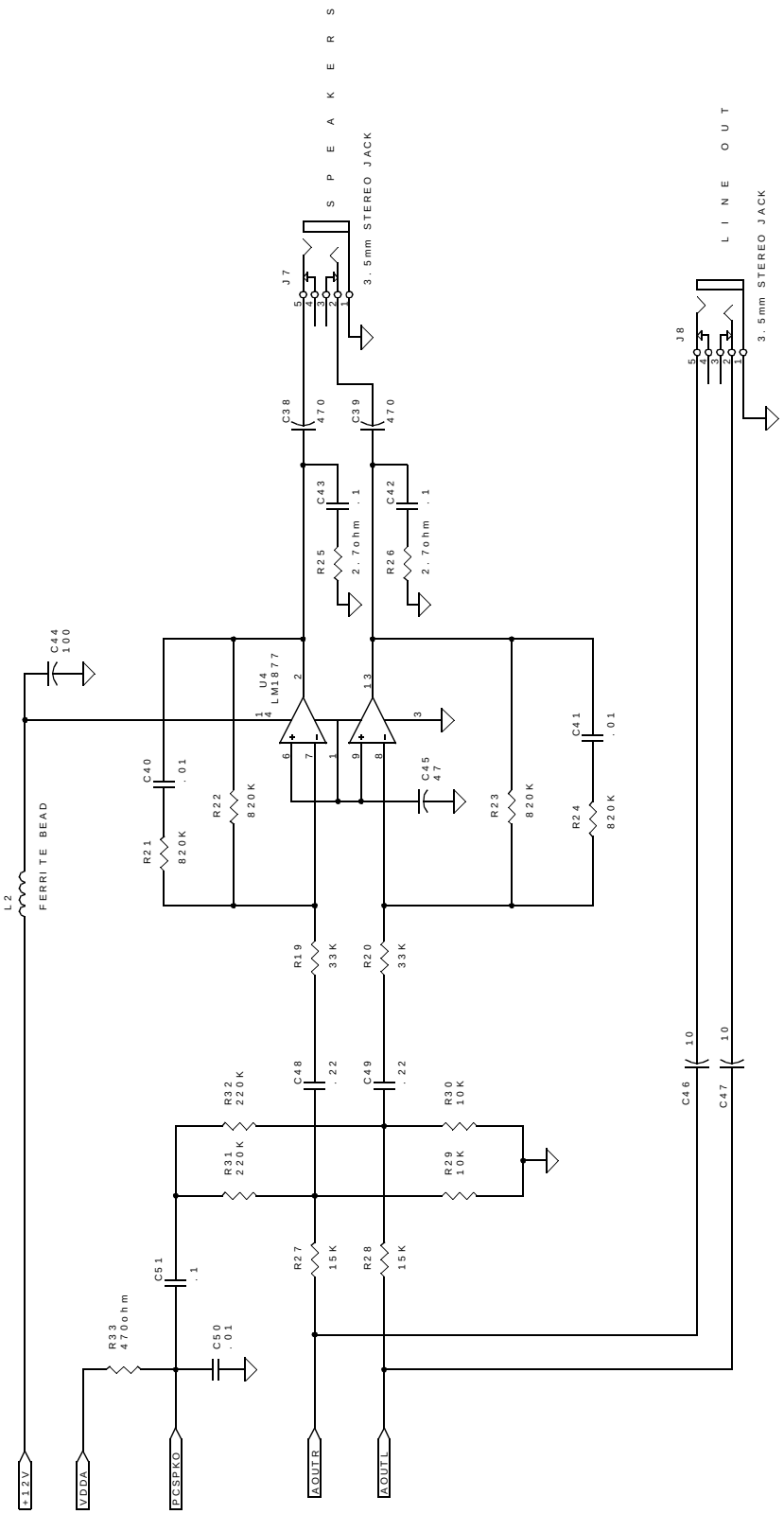


Figure 13 Amplifier Section

APPENDIX C: BILL OF MATERIALS

Table 10 ES1887 Schematics Bill of Materials (BOM)

Item	Quantity	Reference	Part
1	14	C1,C2,C3,C4,C7,C8,C14, C19,C26,C27,C37,C42,C43, C51	.1 µF C805
2	2	C5,C6	22 pF C805
3	8	C9,C10, C24,C25,C46,C47,C52,C53	10 µF .100 Radial
4	10	C11,C12,C13,C15,C16,C17, C20,C21,C48,C49	22 pF C805
5	2	C18, C45	47 µF .100 Radial
6	3	C22,C23,C54	.001 µF Radial
7	1	C28	150 pF C805
8	11	C29,C30,C31,C32,C33,C34C35,C36,C40,C41,C50	.01 µF C805
9	2	C38,C39	470 µF .180 Radial
10	1	C44	100 µF .100 Radial
11	1	D1	1N4148
12	5	JP1,JP2,JP3,JP4,JP5	3P SMD
13	1	J1	13x2 HEADER
14	1	J2	DB15S
15	1	J3	4 HEADER
16	1	J4, J5, J7, J8	3.5mm Stereo Jack
17	1	J6	2x1 HEADER
18	1	J9	IBM J1
20	1	J10	IBM J2
21	1	Q1	Ferrite bead
22	2	R1,R2	7.5k R805
23	10	R3,R4,R5,R6,R7,R8,R9,R10,R11,R12	2.2k R805
24	1	R13	22k R805
25	4	R14,R15,R16,R17	1M R805
26	4	R18,R29,R30,R35	10k Stereo Pot
27	2	R19,R20	33k R805
28	4	R21,R22,R23,R24	820k R805
29	2	R25,R26	2.7 ohm
30	2	R27,R28	15k R805
31	2	R31,R32	220k R805
32	1	R33	470 ohm
33	1	R34	100k R805
34	3	S1,S2,S3	SW Pushbutton
35	1	U1	78L05 TO-92
36	1	U2	ES1887 QFP100
37	1	U3	74LS138
38	1	U4	LM1877
39	1	Y1	14.318MHz Crystal

APPENDIX D: LAYOUT GUIDELINES

PCB Layout

Notebook, Motherboard, Pen-based, and PDA portable computers have the following similarity in PCB layout design:

1. Multi-layer (usually 4 to 8 layer).
2. Double-sided SMT.
3. CPU, core logic (chip set), system memory, VGA controller, and video memory reside in the same PCB.

This is a very noisy environment for adding an audio circuit. The following are the guidelines for PCB layout for an ESS *Audio***Drive**® chip application.

Component Placement

The audio circuit-related components, including the audio I/O jack and connector, must be grouped in the same area.

There are two possible placements for these audio components:

A grouped on one side of the PCB.

B separated on both sides of the PCB.

In Case B, audio component grouping will take less space.

Analog Ground Plane

Audio circuits require two layers of analog ground planes for use as shielding for all analog traces.

In component placement case A (Figure 14), the first layer of analog ground plane is on the analog component side, the second analog ground plane is on the inner layer, and the analog traces are embedded between these two planes.

In component placement case B (Figure 15), the analog ground planes are on both sides of the PCB, and the analog traces are shielded in the middle.

Case A:

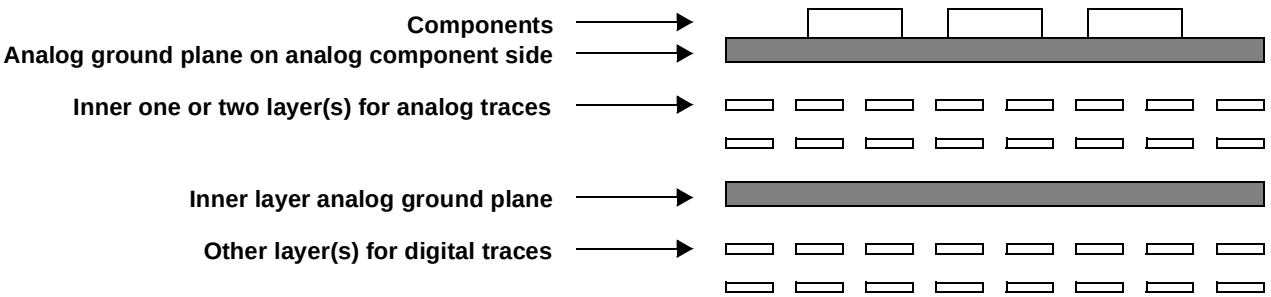


Figure 14 Analog Components on One Side of the PCB

Case B:

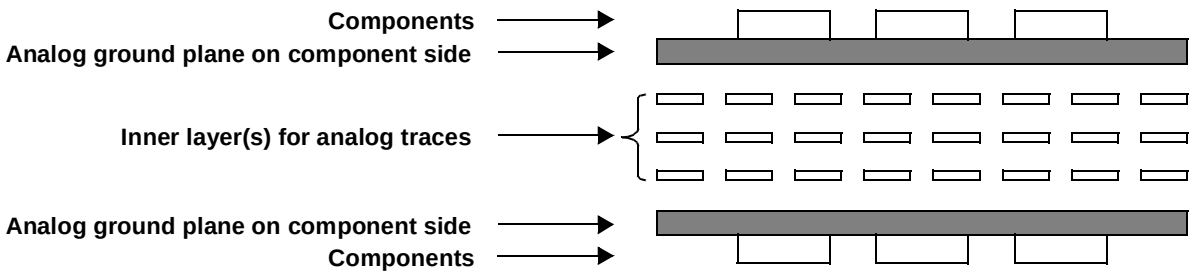


Figure 15 Analog Components on Both Sides of the PCB.

Special Notes

The analog traces should be placed as short as possible.

The MIC-IN circuit is the most sensitive of the audio circuits, and requires proper and complete shielding.

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